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Digital Current Mode Control Algorithms for High-Power Half-Bridge DC/DC Converters

Abstract. *Digitally controlled systems have many well known advantages in comparison to analogue systems e.g. programmability, higher flexibility and modularity, fewer components, lower sensitivity to noise and environment conditions. Theoretically, all analogue control algorithms can be digitalized. But from practical point of view the digitalization often ends up with some major difficulties, which will noticeable limit or even prevent the application of the digital control algorithm. In this paper some of the problems connected to the digitalization are discussed and solutions are proposed. As a result, two new digital current mode control algorithms for high-power, high-voltage half-bridge DC/DC converters are proposed, simulated and experimentally verified.*

Streszczenie. *Cyfrowe systemy sterowania posiadają liczne znane zalety w porównaniu z systemami analogowymi, np. programowalność, wyższą elastyczność funkcjonalną i modułowość budowy, mniejszą liczba komponentów oraz wrażliwość na warunki otoczenia. Teoretycznie wszystkie algorytmy analogowe można zdigitalizować, lecz z praktycznego punktu widzenia często wiąże się to z istotnymi trudnościami, ograniczającymi lub nawet uniemożliwiającymi stosowanie algorytmu cyfrowego. W artykule omówiono niektóre problemy związane z digitalizacją oraz przedstawiono sposoby ich rozwiązania. Zaproponowano dwa nowe cyfrowe algorytmy sterowania wysokonapięciową półmostkową przetwornicą DC/DC, zweryfikowane symulacyjnie i eksperymentalnie.* (***Cyfrowe algorytmy sterowania półmostkowych przetwornic DC / DC dużej mocy ze sprzężeniem prądowym***).

Keywords: digital current mode control, average current mode control, peak current mode control, digital control systems, half-bridge converters.
Słowa kluczowe: sterowanie cyfrowe ze sprzężeniem prądowym, sterowanie ze sprzężeniem względem wartości średniej prądu, cyfrowe systemy sterowania, przekształtniki półmostkowe.

Introduction

The last ten years in power electronics have seen only minor changes and novelty in the field of converter topologies. On the other hand, developments in semiconductor components have been tremendous. Thus, modern trends in power electronics are directed to the implementation of well-known topologies rather than developing new ones. Using new state of the art components, conventional converter topologies can be used more efficiently and for much higher power levels. The recent efforts in the field of power electronics semiconductors are especially interesting for high-power (HP) and high-voltage (HV) applications where the voltage blocking capability of components has always been a major issue. In order to achieve the needed voltage blocking capability traditionally many low voltage components are connected in series but, as a result, the number of components and the complexity of a control system will increase, which reduces the efficiency and overall reliability of the converter. Using new generation components the efficiency and the power density of electronic converters and thus, the feasibility of the whole system can be enhanced.

Rolling stock applications are a good example where recent achievements of power electronics could be introduced. Regarding to the specific design rule, converters based on the IGBT technology for the catenary voltages of 3.0 kV DC are only possible with IGBTs with the blocking voltage not lower than 6.0 kV. The state of the art 6.5 kV IGBT modules (EUPEC, ABB, IXYS, DYNEX, etc.) recently implemented are basically designed for 3.0 kV DC rolling stock applications with their high demands on reliability concerning thermal cycling capability. Single HV IGBT has the voltage blocking capability two times the nominal catenary voltage level, which copes with the requirements for the rolling stock power electronics. Such transistors offer an attractive possibility to avoid series connection of IGBTs (for proper blocking voltage), providing higher efficiency, power density and reliability than the combined HV switch designs. Thus, the concept of 50 kW rolling stock high-voltage high-power half-bridge DC/DC converter was developed and implemented at the Department of Electrical Drives and Power Electronics of Tallinn University of Technology (Fig. 1, Table 1). Based on simple two-level half-bridge topology with state-of-the-art 6.5 kV/200 A IGBTs, the DC/DC converter has shown an outstanding performance as well as light weight and excellent compactness [1].

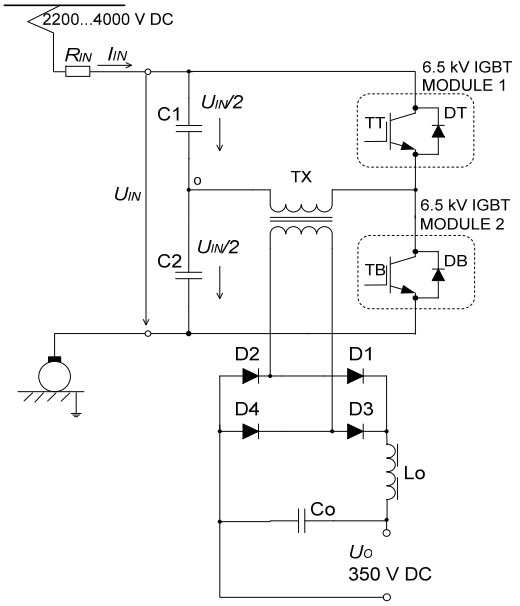


Fig.1. Power circuit of the high-voltage high-power half-bridge DC/DC converter

Table 1. General specifications of the converter

Parameter	Value
Nominal input voltage U_{in}	3.0 kV DC
Minimal input voltage $U_{in,min}$	2.2 kV DC
Maximal input voltage $U_{in,max}$	4.0 kV DC
Nominal output voltage U_O	350 V DC
Rated output power P_O	50 kW
Primary inverter switches (T_T, T_B)	2 x 6.5 kV 200 A IGBT (INFINEON FZ200R65KF1)
Switching frequency f_{sw}	1000 Hz

Given paper discusses two digital current mode control (CMC) algorithms suitable for the proposed half-bridge (HB) DC/DC converter: peak current mode control (PCMC) and average current mode control (ACMC). The algorithms are analysed in detail, benefits and drawbacks are pointed out. Finally, two new improved digital CMC algorithms are proposed and experimentally validated.

Peak Current Mode Control (PCMC)

PCMC regulation loop for the HB DC/DC converter is shown in Fig. 2. It consists of two control loops, inner current and outer voltage control loop. The current peak value (I_{peak}) is adjusted by the outer voltage control loop, which starts with the output voltage (U_{out}) measurement. A regulator (*REG*) eliminates the regulation error and outputs peak current value. Since transformer current ($I_{Tr\text{-}p}$) is alternating current, it is also required to define a negative I_{peak} value. That will be used to control the transistor T_B. The inner current control loop starts with the transformer primary current ($I_{Tr\text{-}p}$) measurement. Comparators (*CP1*, *CP2*) compare the primary current with I_{peak}. When both currents become equal, a RS-latch will be reset and the corresponding transistor will be switched off. The RS-latches are clocked with phase shifted pulses that guarantees 180 º phase shift between control signals. The inner current control loop provides a very fast acting line regulation and overcurrent protection function. The voltage control loop is much slower, depending on the electrical circuit and the regulator time constants hence the response to load variations (which depends on the voltage control loop) will not be as fast as the inherent input voltage transient rejection performance.

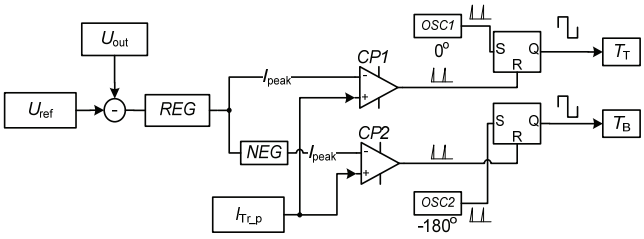


Fig. 2. PCMC principle for the half-bridge DC/DC converter

However, the PCMC cannot be directly applied on a HB DC/DC converter topology due to the possible capacitor voltage unbalance issue, which leads to the transformer volt-second unbalance and saturation. In order to study the influence of the volt-second unbalance on the HB DC/DC converter output, a computer model was created, as shown in Fig. 3. State graphs were used to simulate the PCMC algorithm. Since there are two transistors, there are also two identical state graphs.

Since PCMC algorithm without output voltage compensation loop was applied, line regulation was chosen. This means that the input voltage will be changed, while the load remains constant. The simulation results are presented in Fig. 4. At the beginning the input capacitors (C_1, C_2) are charged equally to the half of the input voltage. The voltage of C_1 gradually starts to increase, while the voltage of C_2 decreases. After 5 ms the input voltage of the converter starts to change, as indicated in Fig. 4*a*. It was found that variable input voltage speeds up the unbalance process and the voltage asymmetry will grow even faster. The load voltage remains stable at the beginning but later if the asymmetry has exceeded a certain limit, also the output voltage will collapse, as shown in Fig. 4*b*. According to (1) the duty cycle of T_T starts to decrease and the duty cycle of the opposite transistor T_B starts to increase. Finally, T_T reaches its minimum duty cycle and T_B the maximum duty cycle, as presented in Fig. 5.

$$t_{on} = L \cdot \frac{\Delta I_{IGBT}}{U_{c2}}. \tag{1}$$

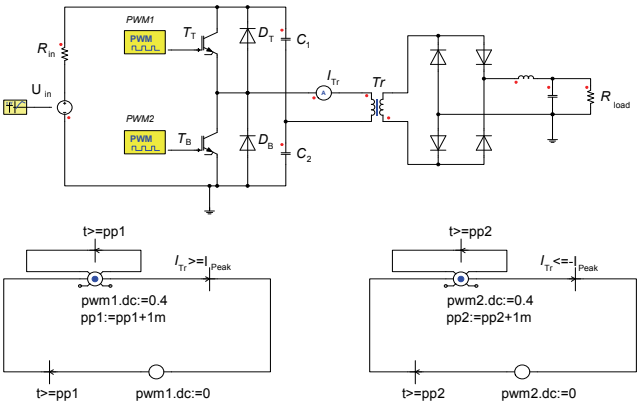


Fig. 3. Computer model of PCMC without outer voltage control loop

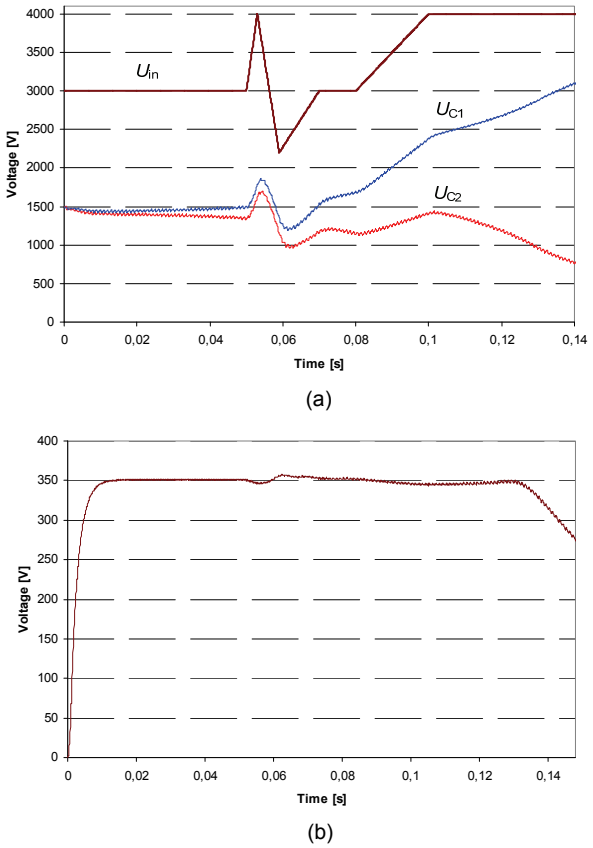
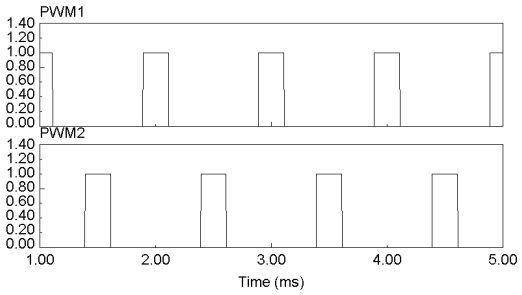


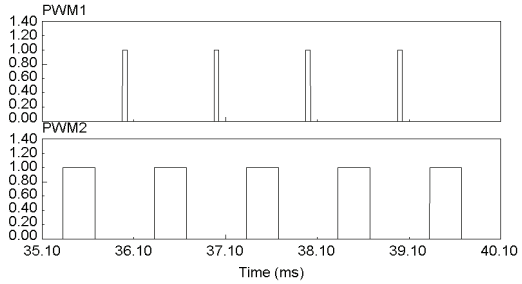
Fig. 4. Volt-second unbalance caused by PCMC: input voltage and unbalanced input capacitors (a), output voltage (b)

There are several possibilities to solve the volt-second unbalance problem inherent to the PCMC. The most common solution is to add a separate winding to the transformer and two catching diodes parallel to the input capacitors [2]. An interesting method of balancing the input capacitor voltage with an additional voltage compensation loop was proposed in [3]. Although this method requires no additional hardware and can be implemented within the software, it still makes the software much more complicated. A similar method was discussed in [4]. The problem could be solved by adding a square wave

compensating signal the amplitude of which is proportional to the voltage unbalance, to the peak current value.



(a)



(b)

Fig. 5. Pulse width signals: at the beginning of the simulation (a) and at the end of the simulation (b)

New Improved PCMC Algorithm with Volt-Second Unbalance Elimination

In this paper a new digital PCMC algorithm is proposed by the authors, which reduces needed current measurement cycles and eliminates volt-second unbalance problem. The proposed idea is to measure just the positive primary current values i.e. the current through the IGBT T_T. The on state time of T_T will be measured and also used for T_B. That way symmetrical control of the HB would be guaranteed and also no voltage unbalance problem of input capacitors could occur since the duty cycle of both transistors is artificially kept equal.

Digital control is based on interrupts. Interrupts offer an excellent possibility to stop the main program at any time instant thus time intervals between interrupts can be adjusted with timers and kept constant. This possibility is useful when applying a digital regulator. Normally there are many interrupt sources that can also occur simultaneously. Carefully planning the timings and priorities of interrupts can avoid overlapping. An interrupt timing diagram is shown in Fig. 6.

Interrupts can suspend the main program at any instant. In the proposed improved peak CMC, two interrupts (Int 1 and Int 2) are used that are triggered by the period match of the corresponding PWM timer, as indicated in Fig. 6. The general control algorithm is shown in Fig. 7. The algorithm is simplified by omitting the outer voltage loop. When an interrupt occurs, the corresponding interrupt routine will be started. The interrupt routine switches on a general purpose timer (GPT), which is used to measure on-state time of the corresponding IGBT. Then the transistor is turned on. The top transistor T_T remains conducting until one of the following conditions is fulfilled: $I_{Tr\text{-}p}$ has reached I_{peak} value or the on-state time ($t_{on\text{-}T}$) has exceeded the maximal allowed conduction time ($t_{on\text{-}max}$). If one of the two conditions is true, T_T is turned off and GPT_1 stopped. The resulting conduction time of T_T is stored for the following interrupt Int 2. The bottom transistor T_B remains conducting until its on-state time is equal to $t_{on\text{-}T}$.

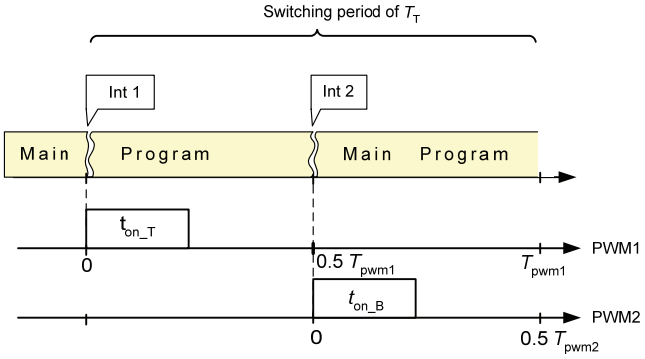


Fig. 6. Interrupt timings for improved PCMC algorithm

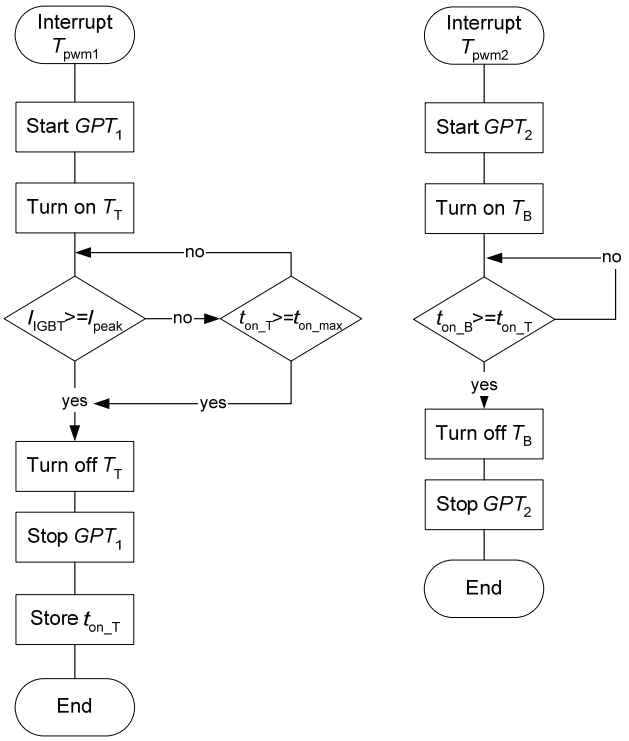


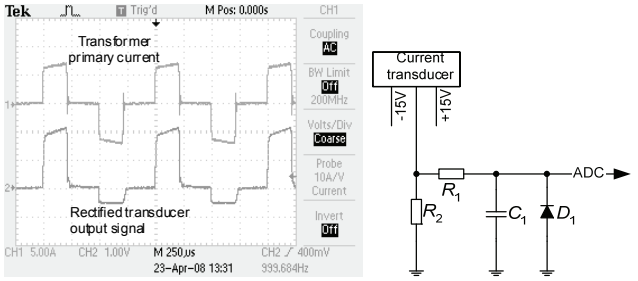
Fig. 7. Improved PCMC algorithm

Experimental results

The primary current of the transformer is an AC current, as shown in Fig. 8*a*. According to the proposed control algorithm, only positive values of the transformer current should be measured. In the case of a current transducer a simple diode rectifier combined with a RC filter can be used, as shown in Fig. 8*b*. Peak CMC is highly sensitive to noise thus correctly dimensioned filter is vital. In Fig. 9 the transducers output signal with and without RC filter are shown. As it can be seen, the filter substantially improves the signal quality.

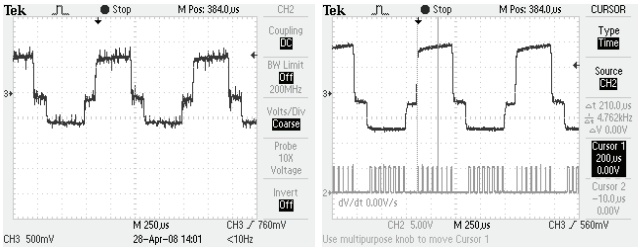
Considering the facts that the voltage unbalance problem could be solved completely within the software without any additional hardware and the number of needed current measurement cycles was reduced, the proposed control method may look as a quite attractive solution for HP and HV applications. However, the resolution issue inherent to all digital control systems, still remains. The accuracy of the current measurement depends on the system clock frequency and A/D conversion speed. As a result also the maximal switching frequency of the converter will be limited. Moreover, high speed current measurement and A/D conversion essentially decrease the overall performance capability of a control unit. Considering the

fact that modern HP and HV DC/DC converters have usually highly complicated control systems, where not only current needs to be measured, one may face the fact that one control unit is not enough to implement digital PCMC.



(a) (b)

Fig. 8. Primary current of the transformer and output signal of a current transducer (a), schematic of current transducer output signal rectifier and filter (b)



(a) (b)

Fig. 9. Output signal of the current transducer without the RC filter (a) output signal with the filter (b)

Average Current Mode Control (ACMC)

The ACMC is a typical two loop control algorithm (inner current loop, outer voltage loop), as shown in Fig. 10. Most of the problems of the peak current mode control are solved in ACMC. Since average current is measured, the control method is less susceptible against noise, the implementation of current error amplifier gives high current loop gain, in the output a regular pulse width modulator is used, which guaranties equal pulses for both transistors. This also eliminates volt-second unbalance problem.

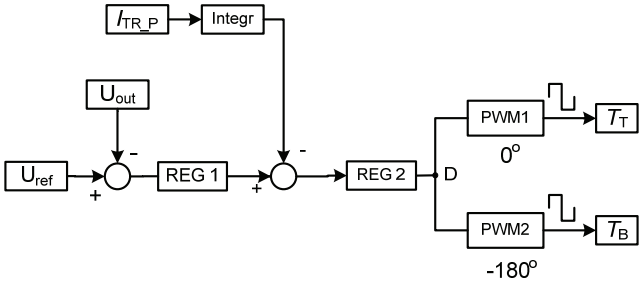


Fig. 10. ACMC principle for the half-bridge DC/DC converter

Digital ACMC can bring some more advantages. A control unit carries out the entire control method in software. Thus, the component number is considerably reduced, there is no ageing or drift of the components, the control system is reprogrammable, which makes the system more adaptable. Also, a variety of adaptive control schemes are possible. Digital ACMC eliminates the gain restrictions of the current error amplifier and increases immunity against EMI. The biggest drawback of digital control is the need to sample and quantize parameters. It introduces a noticeable phase lag to the system and reduces measurement accuracy [5]-[7]. In order to increase the accuracy, sample rate has to be increased. Sample rate is directly connected to the clock frequency of the control unit and cannot be increased endlessly. On the other hand, increasing the sampling rate can overload the control unit, which would reduce the overall performance of the system. In order to sustain the performance of a complex control system several control units may be necessary. Therefore classical approach of digital AVCMC is not an optimal solution for a modern HP and HV DC/DC converter.

New Improved ACMC Algorithm with Reduced Sample Rate of Current Measurement

In the current research project a new mathematical method for a digital ACMC for HB DC/DC converters was developed that allows reducing the sample rate of current measurement without resulting penalties in accuracy. The central idea is to exploit the linear nature of the current slopes. Instead of sampling and summing the inductor current over the switching period, the current is measured only twice per period. The method is based on the digital ACMC described in [8]. The described method is applicable only for buck, boost and flyback topologies while the method proposed here can be applied on two level half-bridge and full-bridge (FB) converter topologies.

HB or FB DC/DC converters have one distinctive difference from simple buck and boost topologies. They have an isolation transformer (Fig. 1) and instead of the inductor current the transformer primary current is measured. In order to calculate average value, the current must be rectified, which is not easy to do in HV and HP applications [3]. Here another simpler method is proposed. Instead of primary current, the IGBT current (I_{IGBT}) is measured. In the case of symmetrical PWM control the average switch current is proportional to the rectified average primary current. The average current ($I_{IGBT\text{-}AV}$) through the respective inverter switch in the HB topology is

$$I_{IGBT\_AV} = \frac{1}{T}\int_{t_1}^{t_2} I_{IGBT}(t)dt \,, \tag{2}$$

where T is the switching period, t_1 is the turn-on instant of a transistor, and t_2 is the turn-off instant of a transistor [9].

The rectified average current of the isolation transformer primary is

$$I_{Tr\_p\_AV} = \frac{2}{T}\int_{t_1}^{t_2} I_{IGBT}(t)dt \,, \tag{3}$$

As it can be seen, $I_{IGBT\text{-}AV}$ is twice lower than $I_{Tr\text{-}p\text{-}AV}$. Due to the symmetry it is irrelevant which current of both transistors will be measured.

The central idea of the proposed digital ACMC method is to measure I_{IGBT} only twice per switching period at the following instants: at the beginning of on-state time (I_1) and at the end of on-state time (I_2) of the IGBT, as shown in Fig. 11. This control method assumes that the current slopes are linear.

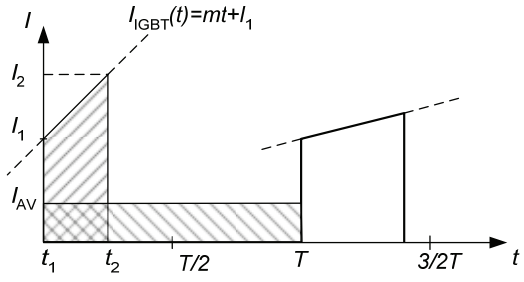


Fig. 11. Idealized IGBT current waveforms in a half- or full-bridge converter

Then an average IGBT current can be easily calculated according to two measured current values. Since the current is always increasing linearly, the current function can be expressed with the linear equation as follows:

$$I_{\mathrm{IGBT}}(t) = m \cdot t + I_1 , \tag{4}$$

where m is the slope of the IGBT current $I_{\mathrm{IGBT}}(t)$, t is time and I_1 is the IGBT current at the beginning of the on-state time. The current slope can be calculated as follows:

$$m = \frac{I_2 - I_1}{t_2 - t_1} , \tag{5}$$

where I_2 is the current value at the end of the on-state time, and I_1 is the current at the beginning of the on-state time. A change in the duty cycle results in a change in the current slope. However, the current retains its linearity. The average current can be found by solving the following integral:

$$\begin{aligned} I_{\mathrm{IGBT\_AV}} &= \frac{1}{T_{\mathrm{PWM}}} \int_{t_1}^{t_2} I_{\mathrm{IGBT}}(t)dt = \frac{1}{T_{\mathrm{PWM}}} \int_{t_1}^{t_2} (m \cdot t + I_1)dt = \\ &= \frac{1}{T_{\mathrm{PWM}}} \left[\int_{t_1}^{t_2} m \cdot t dt + \int_{t_1}^{t_2} I_1 dt \right] = \\ &= \frac{1}{2T_{\mathrm{PWM}}} \cdot (t_2 - t_1) \cdot (I_2 + I_1) , \end{aligned} \tag{6}$$

where $I_{\mathrm{IGBT\text{-}AV}}$ is the average IGBT current, T_{PWM} is the switching period of transistors. In the AVCMC, fixed frequency PWM control is used. Therefore the switching period and the duty cycle are known parameters. By measuring the current at the beginning and at the end of the IGBT on-state time, the average current can be calculated according to (6). However, one must consider that the current shape indicated in Fig. 11 is ideal. The real current shape of a HB converter includes overcurrent peaks at every turn-on instant and depending on the measurement equipment used, can have other abnormal components in the signal.

In order to achieve accurate timing of the digital regulator and synchronize it with other internal processes, interrupts were used. The interrupt timing diagram of the proposed digital AVCMC is shown in Fig. 12. The first interrupt (Int 1) is triggered by period match of the first PWM timer. The IGBT1 current I_1 is measured. The trigger sequence and duration of an interrupt routine are constant values. The duration of the interrupt routine depends on many factors like ADC speed, program structure etc. To avoid interrupt overlapping, the maximal duration of the first interrupt routine is limited with the minimum on-state time ($t_{\mathrm{on\text{-}min}}$). The second interrupt (Int 2) will be triggered at the end of the duty cycle and the IGBT current I_2 will be measured. Since the duty cycle is changing ($t_{\mathrm{on\text{-}min}}$ … $t_{\mathrm{on\text{-}max}}$), the trigger sequence of the second interrupt is also variable, as shown in Fig. 12. The duration of the interrupt routine is limited and can be calculated as follows:

$$t_{\mathrm{int\,2}} = \frac{T_{\mathrm{PWM}}}{2} - t_{\mathrm{on\_max}} , \tag{7}$$

where T_{PWM} is the switching period of IGBTs, $t_{\mathrm{on\text{-}max}}$ is maximal on-state time of the IGBT. The third interrupt (Int 3), triggered by the period match T_{pwm2} executes a regulator. Since the IGBTs of the opposite branches are switched symmetrically and with the same frequency, the trigger sequence of the Int 3 is constant and equals to the sequence of Int 1. The maximal duration of the third interrupt routine is limited with the half PWM period ($0.5T_{\mathrm{PWM}}$).

A general program structure is shown in Fig. 13. As it can be seen, the most vital functions of the converter (control of IGBTs and protection algorithms) are carried out within the main program. Interrupts are only used for processes that require precise timing. There are three interrupt sources: period match of the first PWM timer (T_{PWM1}), period match of the second PWM timer (T_{PWM2}), and period match of a GPT.

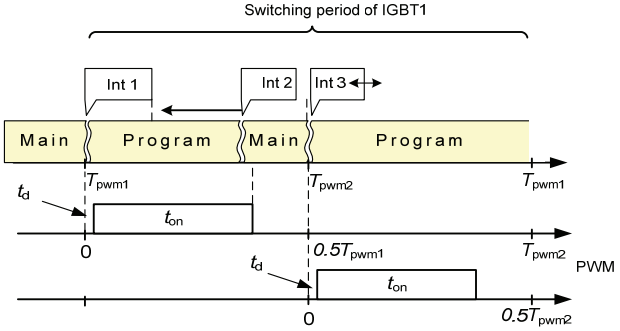


Fig. 12. Interrupt timings of the improved ACMC algorithm

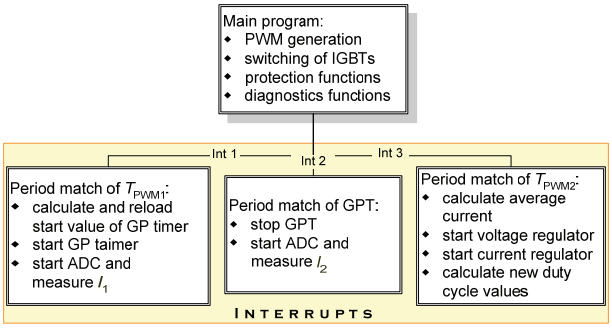


Fig. 13. Program structure diagram of a HB DC/DC converter controlled with the improved ACMC algorithm

The first interrupt service routine (ISR) starts with calculating a new reload value for the GPT, as shown in Fig. 14. The reload value of the GPT is a variable that depends on the current duty cycle. The new value will be reloaded and the GPT started. As a next step, a small pause is generated to compensate the dead time (t_d) added to control signals and also possible current peaks occurring during turn-on. The software delay must be exactly as long as it is needed for the IGBT to fully open and start conducting. Accordingly, ADC is started and after completing the conversion of the IGBT current I_1, ISR returns to the main program.

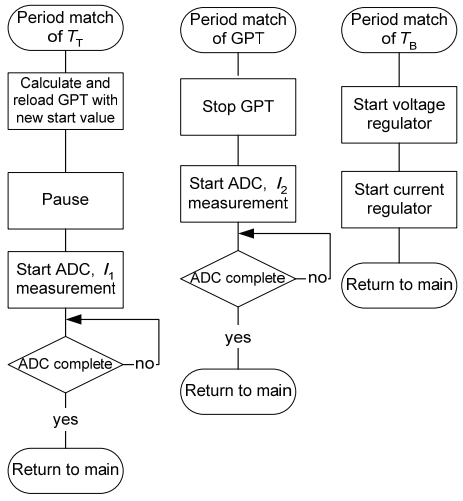


Fig. 14. Flowcharts of interrupt service routines for improved ACMC

The GPT will trigger the next interrupt (Int 2) slightly before turning off the IGBT, as shown in Fig. 12. This guarantees that the current peak is measured before the transistor is turned off and the current decreases to zero. Flowingly, ADC measures IGBT current I_2 and ISR returns to the main program.

The third ISR serves mainly to provide digital regulation and to calculate the new duty cycle for the switches. First, the outer voltage control loop (Fig. 10) provides a new current program for the inner current loop. The inner current control loop then calculates an average current according to (6). A digital current error amplifier (REG2 in Fig. 10) compares the average current to the current program and on that basis calculates new duty cycle *D* for the transistors. The HB is controlled symmetrically and the duty cycles are kept equal to each other.

A drawback of the proposed control method is that it is only suitable for converters where the current is growing linearly. This raises a question of how to build an appropriate converter. In order to answer that question, it is necessary to find out the parameters that the current depends on. In the CMC, the current is measured. Depending on the topology, it can be an inductor or a transformer primary current. The current slope through an inductor or a transformer primary can be calculated as follows:

$$\frac{di}{dt} = \frac{U}{L}, \tag{8}$$

where *di/dt* is the current slope, *U* is the voltage across the winding, and *L* is the inductance of the winding. The digital AVCMC proposed in this paper assumes that the current increases linearly over the on state time. The term linearity refers to the constant current slope. According to (8), a constant slope is only achieved if the ratio U/L remains constant. The terminal voltage U of an inductor or a transformer primary depends on the input voltage and on the duty cycle of the converter. The duty cycle is constant over a switching period. The input voltage change during a switching period is usually small so that U can be considered as constant. Also, inductance must remain constant. The inductance of the winding can be calculated as follows:

$$L = \frac{n \cdot \Phi}{i}, \tag{9}$$

where Φ is the magnetic flux through the area spanned by the current loop, *n* is the number of wire turns, and *i* is the loop current. In order to keep the inductance constant, the ratio between the magnetic flux and the loop current (Φ/i) must remain constant. Transformers and inductors with ferromagnetic cores operate linearly as long as the current through them is not large enough to drive their core materials into saturation. Saturation destroys the balance between the flux and the current, resulting in an inductance change. It is clear that one key element to success is an optimally designed transformer or inductor. Main attention here must be paid to the selection of the proper material for the magnetic core and to define an optimal operating flux density to minimize the dimensions and to improve operability and efficiency of the transformer, respectively [10].

Simulations and Experimental Results

The simulations were carried out with the simulation software *Simplorer*. In order to simplify the simulation, ideal semiconductor devices and a non-saturable isolation transformer were used. The IGBTs are controlled with PWM method. The switching frequency is 1 kHz. The input voltage U_{in} is 1 kV. The transformer has the following parameters: a saw tooth generator changes magnetizing inductance 12…100 mH, primary leakage inductance is 30 μH and secondary leakage inductance is 1 μH. The input capacitors C_1 and C_2 are identical. Since the leakage inductance of the primary is negligibly small compared to the magnetizing inductance, it does not affect the current shape. However, increase in the magnetizing inductance decreases the current slope, as shown in Fig. 15. The magnetizing inductance is changing in saw tooth shape while the current increases exponentially.

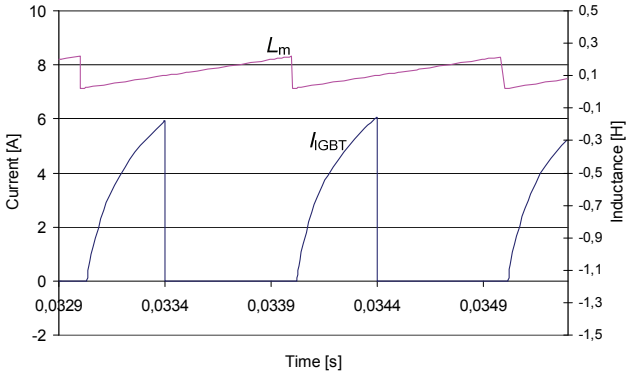


Fig. 15. Variable magnetizing inductance and IGBT current with non-linear slope

In order to demonstrate the influence of the duty cycle on the current shape, following simulations and tests were carried out: without changing any electrical parameters, the duty cycle was reduced from maximum 0.4 to minimum 0.2 resulting in an increase of the current slope, as shown in Fig. 16.

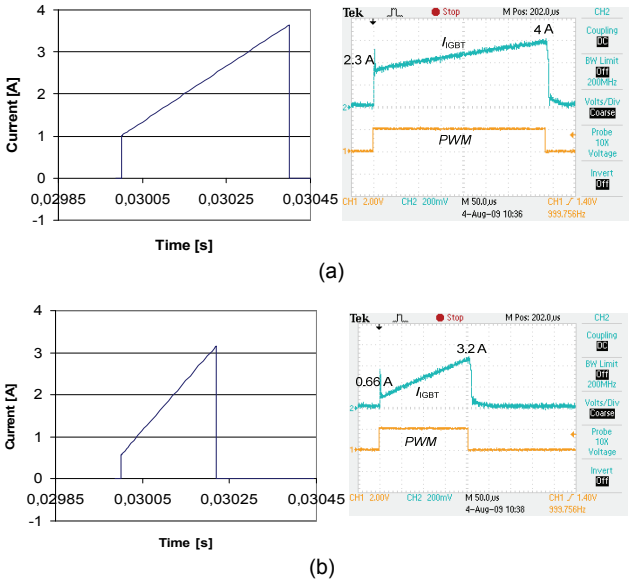


Fig. 16. IGBT current: duty cycle *D*=0.4 (a), duty cycle *D*=0.22 (b)

The accuracy of the proposed control method was verified by importing oscilloscope data into MS Excel where the average current could be calculated using classical integration methods. The current was also calculated using the proposed simplified digital AVCMC equation (6). Comparison of results is shown in Table 2. As it can be seen, in the case of maximal duty cycle the difference between Excel results and those that where obtained with improved AVCMC is only 0.002 A. In the case of minimum duty cycle the difference is slightly bigger 0.004 A.

Table 2. Comparison of results [11]

Duty cycle	**0.4**	**0.22**
Average current with Excel	1.262 A	0.429 A
Average current with Eq. (6)	1.260 A	0.425 A

The proposed digital AVCMC has the following benefits:
- simple equation for average current calculation;
- reduced sample rate, i.e. only two current measurements per duty cycle are needed, resulting in a less loaded microcontroller;

Drawbacks are:
- high speed current measurements required;
- noise susceptibility due to the lower sampling rate.
- applicable only in the case of linear current slope.

Conclusions

Digital control is replacing analogue control in high power and high voltage power electronics converters. This has been a strong tendency over last decade. Modern converters for high power applications are sophisticated systems where high flexibility and compactness is required. Digital control fulfils best those requirements.

The current mode control has very good dynamic response to input voltage and current changes which makes it an attractive algorithm for many power electronics applications. However, implementation of this algorithm in digital control systems has brought up many new difficulties, which are jet to be solved. In this paper two digital current mode control algorithms were studied and main difficulties were pointed out. As a result, two new improved digital current mode control algorithms for high power, high-voltage half-bridge DC/DC converters were proposed, simulated and experimentally verified.

First an improved peak current mode control algorithm specially designed for high power half-bridge DC/DC converters was proposed. The algorithm solves the voltage unbalance problem inherent to the peak current mode control and also reduces the sample rate twice. High power and high voltage power electronics converters typically have relative low operating frequency, which makes the proposed peak current mode control algorithm suitable for such applications.

Secondly new digital average current mode control (AVCMC) method for half-bridge and full-bridge DC/DC converters was proposed. One of the most difficult issues of digital control systems is the resolution of the sample rate. The higher the sample rate of an AD converter, the more accurate the measurement is. On the other hand, increasing the sample rate also increases the load of a microcontroller. Thus, in conventional control systems always a compromise between accuracy and a reasonable load of the microcontroller must be found. The proposed digital AVCMC control method reduces the sample rate to two samples per period without a noticeable loss of accuracy. The control scheme assumes that the transformer primary current is growing linearly and mathematical methods are used to calculate the average current. Conditions for the current linearity were defined. The accuracy of the proposed control method was confirmed by the simulation and measurement results.

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