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Passivity-based Controller Design and Stable Control Region Analysis of the Cascaded DSTATCOM

Abstract. *This paper proposes a novel passivity-based control scheme for the cascaded H-bridge (CHB) DSTATCOM. The mathematical model of the CHB-DSTATCOM is devised by partitioning the CHB-DSTATCOM into n-block subsystems, and the control algorithm is devised using the adaptive passivity controller. The power balancing mechanism and the stable control region are analyzed using the phasorial diagram representation. The Electromagnetic Transient Program (EMTP) is used for digital simulation, and the Transient Analysis of Control System (TACS) and the MODELS language of the EMTP are utilized for control algorithm implementation. The simulation results of the CHB-DSTATCOM under abrupt dc-link voltage variations are provided with comparative evaluations. The devised control scheme of the CHB-DSTATCOM is validated by the simulation and experimental results from the prototype system.*

Streszczenie. *W artykule zaproponowano układ sterowania kaskadowo połączonych systemów DSTATCOM biorąc pod uwagę składowa bierną mocy. Mechanizm równoważenia mocy i sterowanie stabilnością są analizowane na podstawie reprezentacji fazora. (**Bazujący na analizie składowej biernej układ sterowania w systemie kaskadowo połączonych DSTATCOM**)*

Keywords: DSTATCOM, cascaded H-bridge, power balancing, passivity-based controller, electromagnetic transient program (EMTP)
Słowa kluczowe: DSTATCOM, równoważenie mocy, składowa bierna.

I. Introduction

In recent years, the power quality issues have become important topic due to the proliferation of disturbing loads, which causes significant voltage fluctuations, sag/swell and temporary interruptions [1-5]. To mitigate these voltage disturbance problems, the static synchronous compensator (STATCOM) is the most suitable solution, which can be installed at the transmission networks or at the distribution networks to protect the voltage sensitive loads [6-10].

Due to its modularity and flexibility of manufacturing, the cascaded H-bridge (CHB) multilevel inverter configuration is desirable for high-power medium-voltage power quality conditioning applications [7, 8]. However, restricted by the limited switching frequency of the power electronic devices, achieving simultaneous dc-link voltage balancing and sufficient controller bandwidth is rather complicated [10]. This paper aims to provide a systematic procedure for the adaptive controller design of the CHB-DSTATCOM based on passivity control theory, which accounts for the model mismatch and parameter uncertainties. The stable control regions (SCRs) are analyzed using phasorial diagrams. The Transient Analysis of Control System (TACS) and the MODELS language in the EMTP software are adopted to implement the control algorithm. The simulation results and the experimental results from the prototype system are provided for validation of the proposed control algorithm.

The organization of this paper is as follows. Secition II presents the principle of passivity-based controller design method for the CHB-DSTATCOM. Section III presents the power balancing mechanism of the CHB-DSTATCOM, and the stable control regions are analyzed with respect to different dc-link voltage scenarios. Section IV presents the digital simulation results obtained from the Electromagnetic Transient Program-Alternative Transient Program (EMTP-ATP). Next, the experimental results are presented in Section V. Finally, Section VI concludes this paper.

II. Passivity-based Controller Design for the Multilevel CHB-DSTATCOM

Fig.1 shows the circuit diagram of cascaded multilevel DSTATCOM based on *n*-block H-bridge modules. In Figure 1, L_g and R_g indicate the grid impedance. Each H-bridge includes four IGBT switches with anti-parallel diodes and a dc-link capacitor. Thus the output voltages of the CHB-DSTATCOM can be derived as: $v_{aN}=v_{ma1}+\ldots+v_{maN}$.

Assuming $v_{dc,n}=V_{dc}$ (n is integer) in steady state and the unipolar modulation strategy is adopted in PWM process, thus each H-bridge would produce three voltage levels: $-V_{dc}$, 0, V_{dc}. With reference to the upper bridge, it is possible to set $v_{ma1}=+V_{dc}$ by turning on switches S_{11} and S_{14} and $v_{ma1}=-V_{dc}$ by turning on switches S_{12} and S_{13}. Moreover, it is possible to set $v_{ma1}=0$ by turning on either S_{11} and S_{12} or S_{13} and S_{14}, the lower bridge operates in a similar manner. Thus $2n+1$ (n is integer) distinct voltage levels can be synthesized at the ac terminals using n-block inverters. It is worth noticing that, the switching states of S_{x1}, S_{x2} must be complementary to those of S_{x3}, S_{x4} (x=1,…,n) in order to avoid short circuit of the individual H-bridges [4, 6-16, 26].

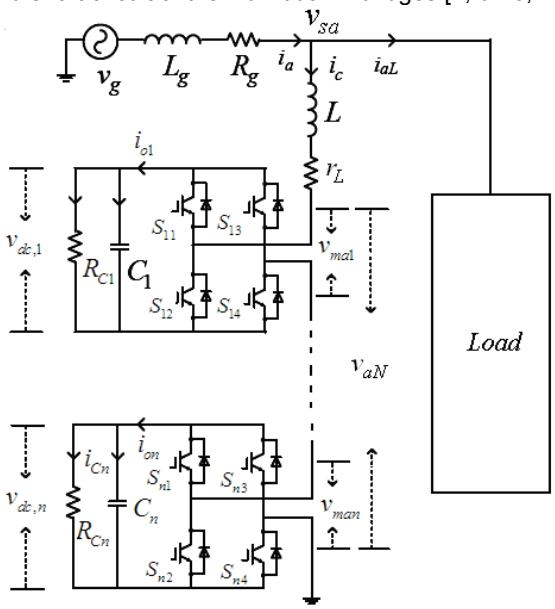


Fig.1 The circuit diagram of the cascaded H-bridge DSTATCOM based on *n*-block modules.

To obtain $2n+1$ (n is integer) level output voltage at the ac terminal, the carrier signals utilized in each cell must be phase shifted by $180/n$ degree in case of n-block H-bridge module configuration. The principle of carrier-shifted pulse width modulation can be found in the previous literatures [6-8, 10, 17]. Moreover, the design guidelines and analysis of the DSTATCOM can be found in references [18-21, 26].

According to the state of the power switches, the system behavior can be described by the following differential equations for i=1, ⋯n.

$$(1) \qquad \dot{i}_c = \frac{1}{L}\left[v_{sa} - r_L i_c - \sum_{i=1}^{n} f_i v_{dc,i} \right], \dot{v}_{dc,i} = \frac{1}{C_i}\left(f_i i_c - g_i v_{dc,i} \right)$$

where g_i is the equivalent parallel conductance for the ith bridge, $g_i = 1/R_{Ci}$, and the switching function f_i (i=1, ⋯n) for each H-bridge can be represented as [17, 22, 26]:

$$(2) \qquad f_i = S_{i1} \times S_{i4} - S_{i2} \times S_{i3}, i = 1,2,...,n$$

where S_{ik} (i=1,...,n; k=1,...,4)∈{0, 1} is the kth switch of the ith H-bridge accounting for the state of the IGBT. And f_i can assume the values {-1;0;1}.

The parameter uncertainties or un-modeled dynamics may cause instability of the whole system, which hampers the practical applications of the multilevel DSTATCOM. By using the passivity-based control method, the energy flow across the individual H-bridge modules is redistributed and the nonlinear damping effect is injected, thus the excellent dynamic characteristics and steady state performance can be ensured. In this paper, the passivity theory and adaptive control scheme is applied to the multilevel DSTATCOM, and the equivalent dc-link resistances are identified in an adaptive manner. Therefore, the asymptotical tracking of the reference currents can be easily achieved [25, 26].

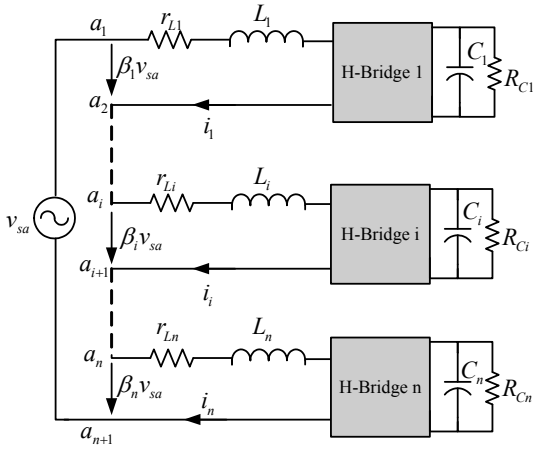


Fig.2 The simplified equivalent circuit of the cascaded APF based on n-block H-bridge modules

To derive the control law based on the passivity theory, the cascaded H-bridge DSTATCOM is partitioned into a n-block subsystem [see Fig.2]. The terminal voltage between a_i and a_{i+1} can be represented as:

$$(3) \qquad v_{ai} - v_{a(i+1)} = \beta_i v_{sa}$$

The following expressions are assumed in order to ensure the equivalence between Fig.1 and Fig.2.

$$(4) \qquad i_1 = i_2 = ... = i_i = ... = i_n = i_c, \sum_{i=1}^{n} \beta_i = 1$$

where the parameter β_i denotes the coefficient which defines the power balancing properties among individual H-bridge inverter modules of the CHB-DSTATCOM.

According to Kirchhoff's law, by setting the current i_c and the dc-link voltages as the state variables, the switching functions of the CHB-DSTATCOM can be derived as:

$$(5) \qquad \begin{cases} L_i \dot{i}_c = \beta_i v_{sa} - r_{Li} i_c - f_i v_{dc,i} \\ C_i \dot{v}_{dc,i} = f_i i_c - g_i v_{dc,i} \end{cases} \quad i = 1,...,n$$

where $L_i = L/n$, $r_{Li} = r_L/n$.

Assuming the grid voltage is denoted by $v_{sa} = V_{sa}\sin\omega_0 t$, and the active component of compensating current i_c is denoted by $i_{ca} = I_{ca}\sin\omega_0 t$, hence the ac-side active power ($P_{in,i}$) and the dc-link active power ($P_{out,i}$) of the ith H-bridge inverter module of the CHB-DSTATCOM can be derived as:

$$(6) \qquad P_{in,i} = \left(I_{cd} \beta_i V_{sa} - r_{Li} I_{ca}^2 \right) \Big/ 2, P_{out,i} = V_{dcref,i}^2 g_i$$

where $V_{dcref,i}$ denotes the reference dc-link voltage of the ith H-bridge inverter unit, according the power balancing mechanism, we get:

$$(7) \qquad P_{in,i} = P_{out,i}$$

Since the resistance r_L is small, the term r_{Li} in Eq.(6) can be neglected, hence the amplitude of active current I_{ca} can be derived as:

$$(8) \qquad I_{ca} = \frac{2 V_{dcref,i}^2 g_i}{\beta_i V_{sa}}$$

From Eq.(8), the following equation can be derived:

$$(9) \qquad \beta_i = \frac{V_{dcref,i}^2 g_i}{V_{dcref,i+1}^2 g_{i+1}} \beta_{i+1}$$

Therefore, the coefficient β_i can be expressed as:

$$(10) \qquad \beta_i = \frac{V_{dcref,i}^2 g_i}{\sum_{i=1}^{n} V_{dcref,i}^2 g_i}$$

Normally, the parameter g_i is unknown under practical situations, which would be estimated by using the adaptive algorithm and the passivity control theory. The tracking error of the current can be denoted as:

$$(11) \qquad \tilde{i}_c = i_c - i_{cd}$$

and the tracking error of the dc-link voltage is denoted as:

$$(12) \qquad \tilde{v}_{dc,i} = v_{dc,i} - v_{dcd,i}$$

Besides, the conductance estimation error is denoted as:

$$(13) \qquad \tilde{g}_i = \hat{g}_i - g_i$$

In Eqs.(11)-(13), i_{cd} and $v_{dcd,i}$ are the estimated values of the actual current i_c and the dc-link voltage $v_{dc,i}$, i.e., $v_{dcd,i} = V_{dcref,i}$, $i_{cd} = i_{ca} + \sum(i_{Lq} + i_{Lh})$, and i_{Lq} and i_{Lh} are the reactive and harmonic component of load current. Besides, $\hat{g}_i$ is the estimated value of the parameter g_i.

According to the passivity theory, the nonlinear damping can be introduced to achieve the predefined steady state and dynamic characteristics. Followed by this principle, the derivative of i_{cd} and $v_{dcd,i}$ can be derived as following equations:

(14) $$\dot{i}_{cd} = \frac{1}{L_i}\left(\beta_i v_{sa} - r_{Li} i_c - f_i v_{dcd,i}\right) + \eta_{1,i}\tilde{i}_c$$

(15) $$\dot{v}_{dcd,i} = \frac{1}{C_i}\left(f_i i_{cd} - \hat{g}_i v_{dcd,i}\right) + \eta_{2,i}\tilde{v}_{dc,i}$$

where coefficients $\eta_{1,i}$ and $\eta_{2,i}$ are damping coefficients, $\eta_{1,i}\tilde{i}_c$ and $\eta_{2,i}\tilde{v}_{dc,i}$ denote the damping quantities injected into the system, and the derivatives of $\tilde{i}_c$ and $\tilde{v}_{dc,i}$ can be derived as:

(16) $$\dot{\tilde{i}}_c = \dot{i}_c - \dot{i}_{cd} = -\frac{1}{L_i} f_i \tilde{v}_{dc,i} + \eta_{1,i}\tilde{i}_c$$

(17) $$\dot{\tilde{v}}_{dc,i} = \dot{v}_{dc,i} - \dot{v}_{dcd,i} = \frac{1}{C_i}\left(f_i\tilde{i}_c - g_i\tilde{v}_{dc,i} + \tilde{g}_i v_{dcd,i}\right) - \eta_{2,i}\tilde{v}_{dc,i}$$

where the term $g_i\tilde{v}_{dc,i}$ denotes damping term. When g_i>0, the stability margin of the whole system increases, and the damping coefficient changes into $g_i/C_i+\eta_{2,i}$, which ensures system stability under a large operation conditions. When g_i<0, the stability margins reduces with the increase of $|g_i|$. Next, the term g_i is estimated using the adaptive law, as:

(18) $$\dot{\hat{g}}_i = \gamma_i(\hat{g}_i - g_{u,i})(\hat{g}_i - g_{d,i})v_{dcd,i}\tilde{v}_{dc,i}, g_{d,i} \le \hat{g}_i(0) \le g_{u,i}$$

where γ_i (γ_i>0) denotes the convergence rate of the adaptive law, and $g_{u,i}$ *and* $g_{d,i}$ defines the upper and lower limits of $\hat{g}_i$. Notably, the inequality $g_{d,i} \le \hat{g}_i \le g_{u,i}$ always holds when g_i>0. From Eqs.(16)-(18), the Lyapunov function can be derived as:

(19) $$\tilde{H} = \sum_{i=1}^{n}\tilde{H}_i = \sum_{i=1}^{n}\left[\frac{L_i}{2}\tilde{i}_c^{\,2} + \frac{C_i}{2}\tilde{v}_{dc,i}^2 + \frac{1}{\gamma_i}\log\left|\frac{\left(\hat{g}_i - g_{u,i}\right)^{\tau_i}}{\left(\hat{g}_i - g_{d,i}\right)^{\tau_i+1}}\right|\right]$$

where τ_i is represented as:

(20) $$\tau_i = \left(g_i - g_{u,i}\right)/\left(g_i - g_{d,i}\right) < 0\,.$$

Furthermore, the derivative of Eq.(19) can be derived as:

$$\dot{\tilde{H}} = \sum_{i=1}^{n}\dot{\tilde{H}}_i = \sum_{i=1}^{n}\left[\begin{array}{l} -\eta_{1,i}\tilde{i}_c^{\,2} - \left(g_i + C_i\eta_{2,i}\right)\tilde{v}_{dc,i}^2 + \\ \tilde{g}_i v_{dcd,i}\tilde{v}_{dc,i} - \dfrac{\tilde{g}_i \bullet \dot{\hat{g}}_i}{\gamma_i\left(\hat{g}_i - g_{u,i}\right)\left(\hat{g}_i - g_{d,i}\right)} \end{array}\right]$$

(21) $$= \sum_{i=1}^{n}\left[\begin{array}{l} -\eta_{1,i}\tilde{i}_c^{\,2} - \left(g_i + C_i\eta_{2,i}\right)\tilde{v}_{dc,i}^2 + \tilde{g}_i v_{dcd,i}\tilde{v}_{dc,i} - \\ \dfrac{\tilde{g}_i \bullet \gamma_i(\hat{g}_i - g_{u,i})(\hat{g}_i - g_{d,i})v_{dcd,i}\tilde{v}_{dc,i}}{\gamma_i\left(\hat{g}_i - g_{u,i}\right)\left(\hat{g}_i - g_{d,i}\right)} \end{array}\right]$$

$$= \sum_{i=1}^{n}\left[-\eta_{1,i}\tilde{i}_c^{\,2} - \left(g_i + C_i\eta_{2,i}\right)\tilde{v}_{dc,i}^2\right]$$

From Eq.(21), it can be noticed that $\dot{\tilde{H}}$ is always semi-negative definite, hence the controller is asymptotically stable in the sense of Lyapunov, regardless of the number (n) of the inverter units. Therefore, the control law can be derived as Eq.(22).

By using the energy re-distribution and damping injection techniques based on the passivity-based control scheme, the stability of the system under a large range of parameter variations can be ensured.

(22) $$\begin{cases} f_i = \dfrac{1}{v_{dcd,i}}\left(\beta_i v_{sa} - r_{Li} i_c - L_i\dot{i}_{cd} + \eta_{1,i}\tilde{i}_c\right) \\ \dot{v}_{dcd,i} = \dfrac{1}{C_i}\left(f_i i_{cd} - \hat{g}_i v_{dcd,i}\right) + \eta_{2,i}\tilde{v}_{dc,i} \\ \dot{\hat{g}}_i = \gamma_i(\hat{g}_i - g_{u,i})(\hat{g}_i - g_{d,i})v_{dcd,i}\tilde{v}_{dc,i} \end{cases}$$

III. Power Balancing Mechanism of the Multilevel CHB-DSTATCOM

In order to analyze power balancing mechanism of the cascaded multilevel DSTATCOM, the two-block system is considered herein for the sake of brevity. The ac-side and dc-side voltages for each inverter module are denoted as:

(23) $$v_{ma1} = f_1 v_{dc,1}, v_{ma2} = f_2 v_{dc,2}$$

where f_1 and f_2 are the switching functions of each inverter unit, according to Kirchhoff's law, the instantaneous power absorbed by the dc-link resistors R_{C1}, R_{C2} are denoted as:

(24) $$p_{R1} = v_{dc,1} i_{R1}, p_{R2} = v_{dc,2} i_{R2}$$

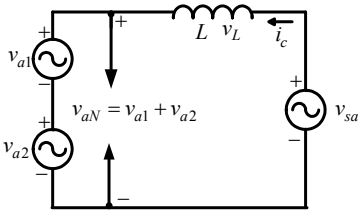
Based on the power balancing mechanism, the following equalities hold:

(25) $$v_{ma1} i_c = C_1\frac{d}{dt}\left(\frac{v_{dc,1}^2}{2}\right) + p_{R1}, v_{ma2} i_c = C_2\frac{d}{dt}\left(\frac{v_{dc,2}^2}{2}\right) + p_{R2}$$

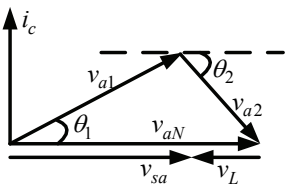
To simplify the analysis, the equivalent resistance across the coupling inductor is neglected. Hence the equivalent circuit diagram of the 2-block system is represented by Fig.3. In Fig.3, each inverter unit is represented as voltage source v_{a1} and v_{a2}, which denote the root-mean-square (RMS) value of the fundamental components of the ac-side output voltages v_{ma1}, v_{ma2}. The output current i_c and the grid voltage v_{sa} are also represented by the RMS values, which are calculated as:

(26) $$x_i = \sqrt{\frac{1}{T}\int_0^T X_{i,1}^2 dt}$$

where x_i denotes the root-mean-square value, $X_{i,1}$ denotes the fundamental component of the voltage or current, T represents the period of fundamental grid voltage.



(a)



(b)

Fig.3 (a) The equivalent circuit of the 2-block cascaded H-bridge DSTATCOM; (b) the phasorial diagram of the voltage and current when i_c is reactive current

As shown in Fig.3(a), the power flow of each inverter unit depends on the angle differences between the injection current i_c and the output voltages v_{a1} and v_{a2}. For the sake of brevity, the current i_c is supposed to be the reactive current, and the power distribution between inverter units is discussed herein. Fig.3(b) shows the phasorial diagram of the inverter current i_c, and the output voltage of the inverter v_{a1} and v_{a2}. The synthesized voltage v_{aN} and grid voltage v_{sa} are also shown. It shows that the compensating current is leading the grid voltage by 90 degrees, and the phase angles between v_{a1}, v_{a2} with grid voltage v_{sa} are denoted by θ_1 and θ_2. The voltage drop across the coupling inductance L is opposite with the grid voltage vector, thus the instantaneous active power P_{a1}, P_{a2} and reactive power Q_{a1}, Q_{a2} can be denoted as [17, 22]:

$$P_{a1} = v_{a1} i_c \sin\theta_1, P_{a2} = v_{a2} i_c \sin\theta_2 \tag{27}$$

$$Q_{a1} = -v_{a1} i_c \cos\theta_1, Q_{a2} = -v_{a2} i_c \cos\theta_2 \tag{28}$$

Therefore, the total active power P_{all} and reactive power Q_{all} of the two H-bridge inverter are represented as:

$$P_{all} = P_{a1} + P_{a2} = i_c \times (v_{a1} \sin\theta_1 + v_{a2} \sin\theta_2) = 0 \tag{29}$$

$$Q_{all} = Q_{a1} + Q_{a2} = -i_c \times (v_{a1} \cos\theta_1 + v_{a2} \cos\theta_2) = -v_{aN} i_c \tag{30}$$

From Eqs.(29)-(30), it can be deduced that there is no active power exchange between the two inverter units. The maximum root-mean-square values of the inverter ac-side output voltages v_{a1m}, v_{a2m} can be represented as [17]:

$$v_{a1m} = \frac{4v_{dc,1}}{\pi\sqrt{2}}, v_{a2m} = \frac{4v_{dc,2}}{\pi\sqrt{2}} \tag{31}$$

The reactive power injected by invdividual inverter unit depends on the inverter dc-link voltage and the modulation signal. To analyze the mechanism of power distribution between each cell, the following conditions are discussed: (1) $v_{a1m} \le v_{aN}$, $v_{a2m} \le v_{aN}$; (2) $v_{a1m} > v_{aN}$, $v_{a2m} \le v_{aN}$; (3) $v_{a1m} > v_{aN}$, $v_{a2m} > v_{aN}$. Notably, the following inequality always holds:

$$v_{a1} \le v_{a1m}, v_{a2} \le v_{a2m} \tag{32}$$

Furthermore, the following inequality is also assumed:

$$v_{a1m} + v_{a2m} \ge v_{aN} \tag{33}$$

A. Power Distribution Mechanism When $v_{a1m} \le v_{aN}$, $v_{a2m} \le v_{aN}$

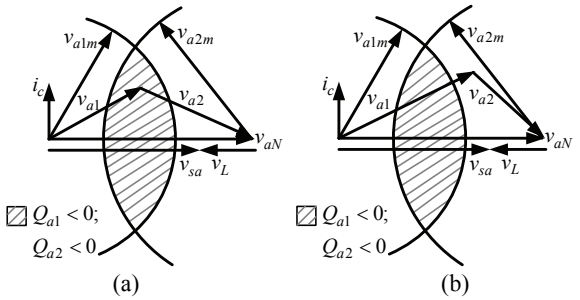


Fig.4 (a) The stable control region (SCR) when $v_{a1m} \le v_{aN}$ and $v_{a2m} \le v_{aN}$ (shadowed area); (b) The unfeasible area when $v_{a1m} \le v_{aN}$ and $v_{a2m} \le v_{aN}$ (excluding the shadowed area)

Fig.4 shows the stable and unfeasible control area when $v_{a1m} \le v_{aN}$ and $v_{a2m} \le v_{aN}$. As shown in Fig.4(a), when the control points locate inside the shadowed area, the vectors of the output voltages v_{a1} and v_{a2} are within circle with the radius of the amplitude v_{a1m} and v_{a2m}, and centered at the terminal of voltage vector v_{aN}. Whereas, it can be observed from Fig.4(b) that, when the control points are outside of the shadowed area, the control is unfeasible. Moreover, it shows in Fig.4 that the projections of the voltage vector v_{a1} and v_{a2} on v_{sa} are always positive, i.e., the two H-bridge inverters inject or absorb reactive power simultaneously. It can also be noticed from Fig.4 that, when one cell of the multilevel inverter absorbs active power, another one generates the equal amount of active power thus the sum of instantaneous active powers $P_{all}=P_{a1}+P_{a2}$ is zero.

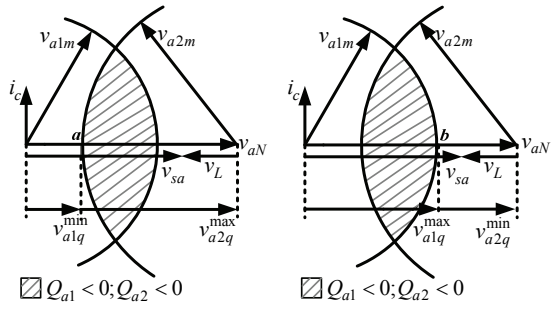


Fig.5 Maximum and minimum active power limits when $v_{a1m} \le v_{aN}$ and $v_{a2m} \le v_{aN}$

Fig.5 shows the vector diagram of the maximum and minimum active power limits under a constant total reactive power Q_{all} when $v_{a1m} \le v_{aN}$ and $v_{a2m} \le v_{aN}$. Fig.5(a) shows the case when voltage v_{a1} has the shortest projection on the voltage vector v_{sa}, hence the first inverter unit injects the minimum reactive power and the second inverter injects the maximum reactive power. Similarly, Fig.5(b) shows the case when voltage v_{a2} has the shortest projection on the voltage vector v_{sa}, hence the first inverter unit injects the maximum reactive power and the second inverter injects the minimum reactive power.

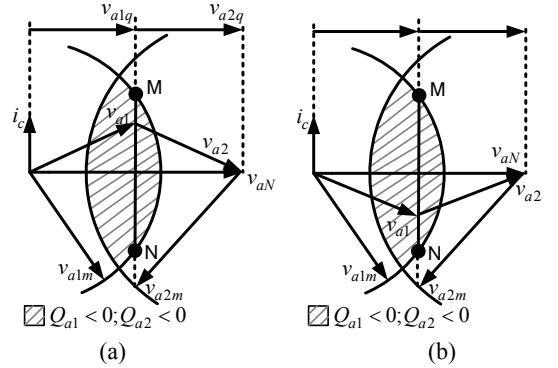


Fig.6 Two possible situations when $Q_{a1}=Q_{a2}$ and $v_{a1m} \le v_{aN}$, $v_{a2m} \le v_{aN}$. (a) The control point locates above v_{aN}; (b) The control point locates under v_{aN}

Fig.6 shows the diagram of two possible situations when the reactive power is equally distributed between the two inverter modules. In Fig.6, the line labeled as 'MN' locates at the center of the voltage vector v_{aN}. Hence any control point in 'MN' satisfies the requirement for equal reactive power sharing among the inverter modules. Fig.6(a) shows the case when the first inverter unit absorbs active power while the second inverter unit injects active power. Fig.6(b) shows the case when the first inverter unit injects active power while the second inverter unit absorbs active power. Notably, in either case, the total active power consumption of the CHB-DSTATCOM is zero when the current i_c is 90 degrees phase shifted with respect to the grid voltage.

B. Power Distribution Mechanism When $v_{a1m}>v_{aN}$, $v_{a2m}\leq v_{aN}$

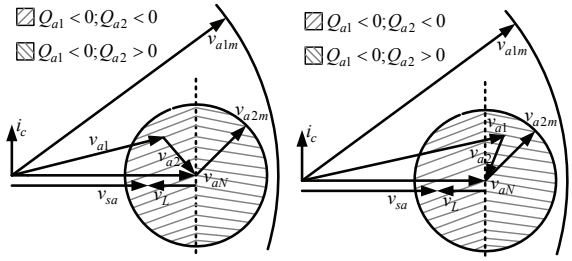


Fig.7 The stable control region (SCR) when $v_{a1m}>v_{aN}$ and $v_{a2m}\leq v_{aN}$. (a) $Q_{a1}<0$, $Q_{a2}<0$; (b) $Q_{a1}<0$, $Q_{a2}>0$.

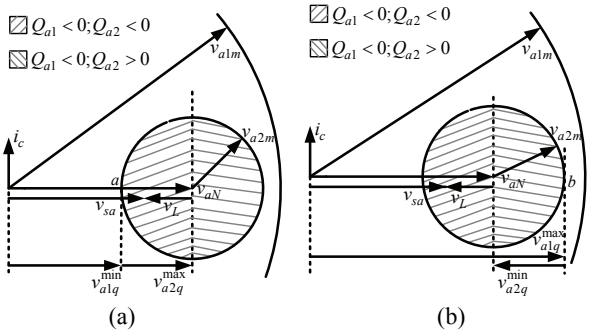


Fig.8 Maximum and minimum active power limits when $v_{a1m}>v_{aN}$ and $v_{a2m}\leq v_{aN}$

When $v_{a1m}>v_{aN}$, $v_{a2m}\leq v_{aN}$, it is possible to synthesize the multilevel output voltage v_{aN} by using both the two inverter units or only using the individual unit with a higher dc-link voltage. Fig.7 shows the two possible phasorial diagrams. When the control points are within the left half plane of the shadowed area in Fig.7(a), the projection of the voltages v_{a1} and v_{a2} into v_{sa} are always positive, i.e., the two cells injects capacitive reactive power to the grid ($Q_{a1}<0$, $Q_{a2}<0$). When the control points are within the right half plane of the shadowed area in Fig.7(b), the first inverter unit injects capacitive reactive power and the second inverter unit injects inductive reactive power, i.e., $Q_{a1}<0$, $Q_{a2}>0$. Notably, when $v_{a1m}>v_{aN}$, $v_{a2m}\leq v_{aN}$ and the total reactive power $Q_{all}<0$, then Q_{a2} can be positive or negative but Q_{a1} is always negative. Meanwhile, the total value of the active power P_{a1} and P_{a2} is always zero, which implies no active power exchange between the multilevel inverter with the grid.

Fig.8 shows the phasorial diagram of the maximum and minimum active power limits under a constant total reactive power Q_{all} when $v_{a1m}>v_{aN}$ and $v_{a2m}\leq v_{aN}$. Fig.8(a) shows the case when voltage v_{a1} has the shortest projection on the voltage vector v_{sa}, hence the first inverter unit injects the minimum reactive power and the second inverter injects the maximum reactive power. Similarly, Fig.8(b) shows the case when voltage v_{a2} has the shortest projection on the voltage vector v_{sa}, hence the first inverter unit injects the maximum reactive power and the second inverter injects the minimum reactive power.

C. Power Distribution Mechanism When $v_{a1m}>v_{aN}$, $v_{a2m}>v_{aN}$

When $v_{a1m}>v_{aN}$, $v_{a2m}>v_{aN}$, it is possible to synthesize the multilevel output voltage v_{aN} by using both the two inverter units or only using the individual inverter unit. Hence three possible operation conditions can be deduced, and the phasorial diagrams with respect to the three conditions are shown in Fig.9.

Fig.9(a) shows the case when the first inverter module injects inductive reactive power and the second inverter unit injects capacitive reactive power, i.e., $Q_{a1}>0$, $Q_{a2}<0$, thus the control points are located at the left hand side of the left dash line. Fig.9(b) shows the case when both of the inverter unit injects capacitive reactive power, i.e., $Q_{a1}<0$, $Q_{a2}<0$, thus the control points are located in the area within the two dash lines. Fig.9(c) shows the case when the first inverter unit injects capacitive reactive power and the second inverter unit injects inductive reactive power, i.e., $Q_{a1}<0$, $Q_{a2}>0$, thus the control points are located at the right hand side of the right dash line. It should be noted that, when condition $v_{a1m}>v_{aN}$, $v_{a2m}>v_{aN}$ are satisfied, the aforementioned three cases in Fig.9 holds when the total reactive power injected to the grid is negative.

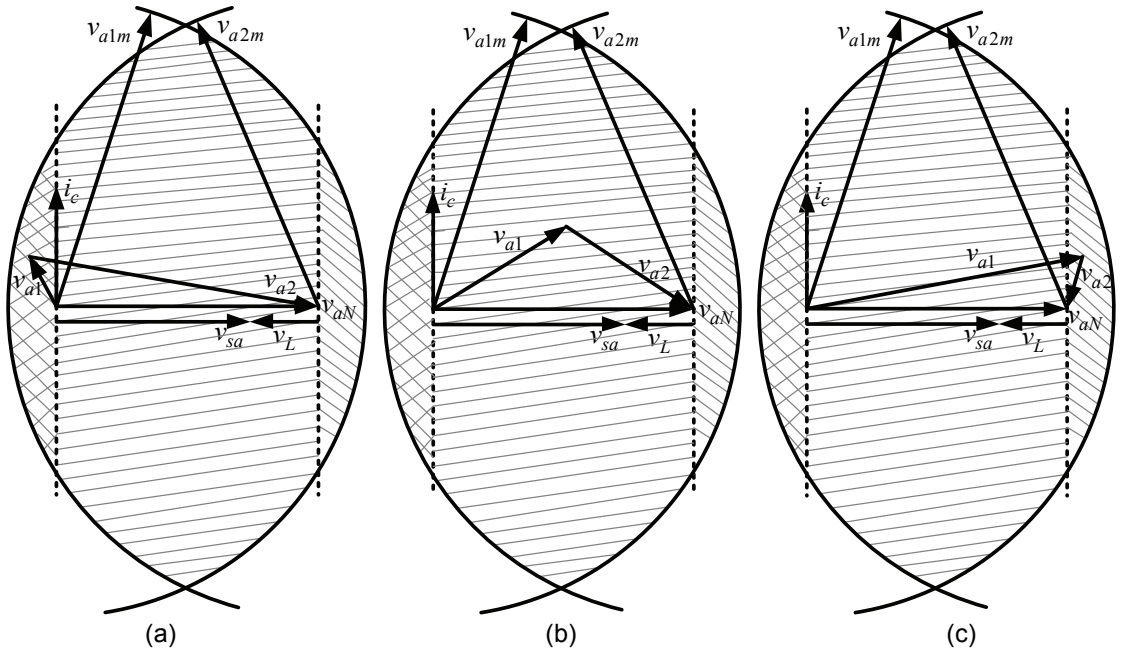


Fig.9 The stable control region (SCR) of the multilevel CHB-DSTATCOM when $v_{a1m}>v_{aN}$ and $v_{a2m}>v_{aN}$

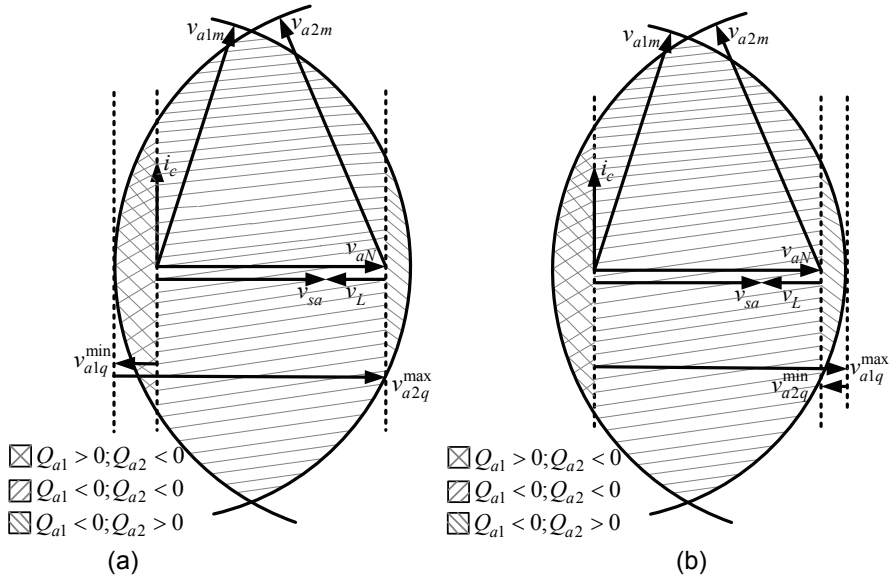


Fig.10 Maximum and minimum reactive power limits when $v_{a1m}>v_{aN}$ and $v_{a2m}>v_{aN}$

Fig.10 shows the phasorial diagram of the maximum and minimum active power limits under a constant total reactive power Q_{all} when $v_{a1m}>v_{aN}$ and $v_{a2m}>v_{aN}$. Fig.10(a) shows the case when the voltage v_{a1} has the shortest projection on the grid voltage vector v_{sa}, hence the first inverter unit injects the minimum reactive power and the second inverter injects the maximum reactive power. Similarly, Fig.10(b) shows the case when voltage v_{a2} has the shortest projection on the voltage vector v_{sa}, hence the first inverter injects the maximum reactive power and the second inverter unit injects the minimum reactive power.

IV.Simulation Results From The Alternative Transient Program-Electromagnetic Transient Program (EMTP)

To validate the effectiveness of the devised control algorithm, the simulation results using the Alternative Transient Program-Electromagnetic Transient Program-(ATP-EMTP) are presented in this section. The circuit parameters are listed as follows: L_g=100μH, R_g=50mΩ, L=2.0mH, r_L=50mΩ, and the inverter dc-link parameters are: C_1=C_2=2500μF, R_{C1}=R_{C2}=20kΩ, and the sampling time T_s=100μs, the grid voltage v_{sa}=220V(rms), the target inverter dc-link voltage is 200V. The load is consisted of a resistance R=4Ω connected in parallel with an inductance L=25 mH.

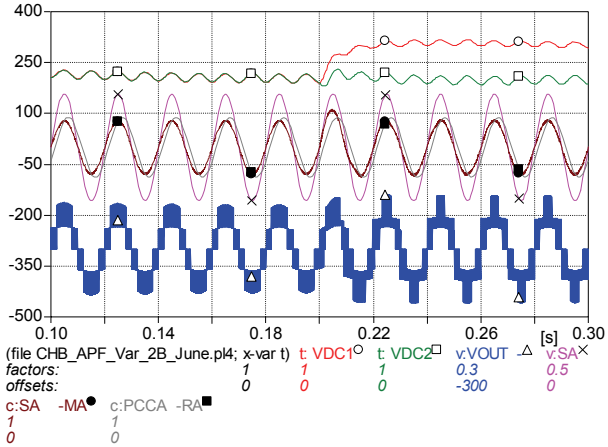


Fig.11 The simulation result of the CHB-DSTATCOM under abrupt changes in the reference dc-link voltage (case 1). ($V_{dc1,ref}$: 200V→300V; $V_{dc2,ref}$: 200V→200V)

The control algorithms are implemented using the built-in function of the Transient Analysis of Control System (TACS), which was introduced in EMTP in 1976 and was initially developed to model controller for the HVDC converters. In the ATP version of the EMTP, the mathematical models can be easily described by using the well-known MODELS language, which provides a description of the structure of a model, and the function of its elements [5, 14-17, 22-26].

Figs.11-14 shows the simulation results of multilevel DSTATCOM under abrupt changes in the reference dc link voltages to verify the validity of the devised control scheme. For the sake of brevity and better illustration, only simulation results of the two cell five-level CHB-DSTATCOM are presented. Notably, in the following simulaton waveforms, the dc-link voltages are denoted as 't:VDC1' and 't:VDC2', the output multilevel voltage is denoted as 't:VOUT', the grid voltage is shown as 'v:SA', the grid current is denoted as 'c:SA -MA' and the load current is denoted as 'c: PCCA -RA'.

To better illustrate the simulation results, the signals are scaled with different scaling factors and offsets. In Figs.11-14, the dc-link voltages of the multilevel inverter are initially set to be 200V, and the reference voltages are abrupted changed at t=2.0s. In Fig.11, the dc-link reference voltages are set as 200V when t<0.2s, the five level terminal voltage are synthesized. The CHB-DSTATCOM generates leading compensation current and the unity power factor (UPF) is achieved at the grid side, and perfect dc link voltage stability is also realized. When t=0.2s, the target dc voltage of the first inverter is set as 300V. It is worth noticing that the condition $v_{a1m}\le v_{aN}$ and $v_{a2m}\le v_{aN}$ holds when t<0.2s, and when t>0.2s, the condition $v_{a1m}>v_{aN}$, $v_{a2m}\le v_{aN}$ holds.

In Fig.12, the dc-link reference voltages are set as 200V when t<0.2s, the five level terminal voltage are synthesized. The CHB-DSTATCOM generates leading compensation current and the unity power factor (UPF) is achieved at the grid side, and perfect dc link voltage stability is realized. When t=0.2s, the target dc voltages are set as 300V and 350V, respectively. Notably, the conditions $v_{a1m}\le v_{aN}$ and $v_{a2m}\le v_{aN}$ holds when t<0.2s, and when t>0.2s, the condition $v_{a1m}>v_{aN}$, $v_{a2m}>v_{aN}$ holds. It shows in Fig.12 that the dc voltages track the reference

in one fundamental period, and the grid voltage and grid current are also in phase with each other. However, the synthesized output voltage reduces to three level. It can be inferred that the stability of the system is ensured at the cost of increased switching ripples and higher EMI.

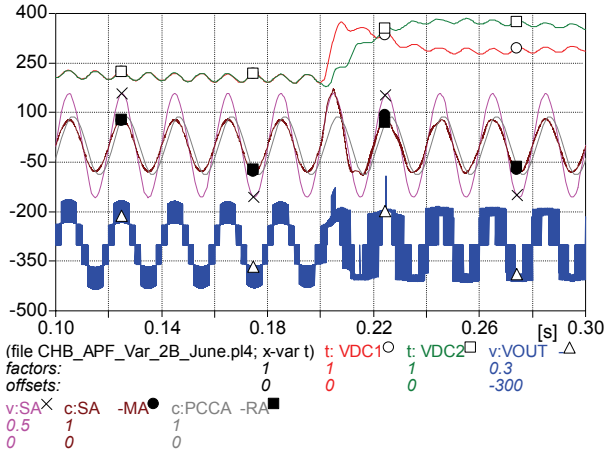


Fig.12 The simulation result of the CHB-DSTATCOM under abrupt changes in the reference dc-link voltage (case 2). ($V_{dc1,ref}$: 200V→300V; $V_{dc2,ref}$: 200V→350V)

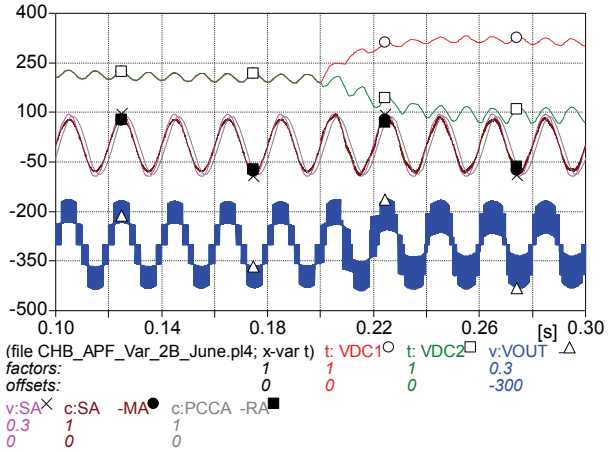


Fig.13 The simulation result of the CHB-DSTATCOM under abrupt changes in the reference dc-link voltage (case 3). ($V_{dc1,ref}$: 200V→300V; $V_{dc2,ref}$: 200V→100V)

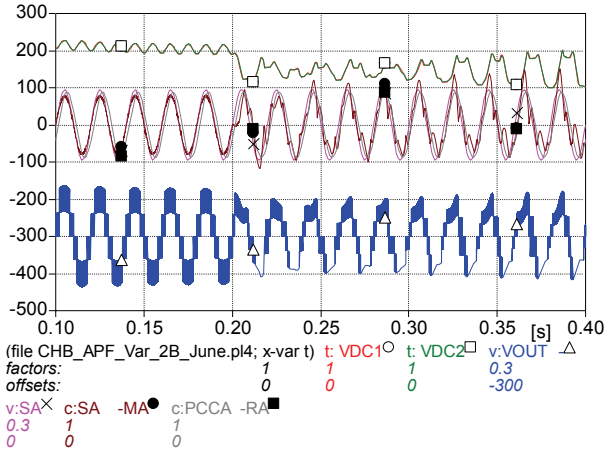


Fig.14 The simulation result of the CHB-DSTATCOM under abrupt changes in the reference dc-link voltage (case 4). ($V_{dc1,ref}$: 200V→100V; $V_{dc2,ref}$: 200V→100V)

Fig.13 shows the simulation results when the dc-link reference voltages are abruptly changed to 300V and 100V at t=0.2s, respectively. Similarly, the conditions $v_{a1m} \leq v_{aN}$ and $v_{a2m} \leq v_{aN}$ holds when t<0.2s, and when t>0.2s, the condition $v_{a1m} > v_{aN}$, $v_{a2m} < v_{aN}$ holds. In Fig.13, the stability of the CHB-DSTATCOM is ensured during dynamic variation of the dc-link voltages, at the tradeoff of the higher switching ripple in the grid current due to the reduced voltage level in the synthesized multilevel output voltage. Fig.14 shows the simulation results when the dc reference voltages are abruptly changed to 100V at t=0.2s. Similarly, the conditions $v_{a1m} \leq v_{aN}$ and $v_{a2m} \leq v_{aN}$ holds when t<0.2s, and when t>0.2s, the condition $v_{a1m} < v_{aN}$, $v_{a2m} < v_{aN}$ holds. However, the dc-link voltages diverge when t>0.2s due to the fact that the condition $v_{a1m}+v_{a2m} \geq v_{aN}$ is violated [see Eq.(33)].

Figs.11-14 shows that the stability of the multilevel CHB-DSTATCOM can be ensured over a wide range of variations in the reference dc-link voltages, both under steady state and dynamic operation conditions. Besides, it is verified that the aforementioned theoretical analysis is quite effective to investigate the mechanism of the dc link voltage stabilization and stable control regions.

V. Experimental Results of the Prototype System

To reconfirm the validity of the devised control scheme, a hardware prototype system is built, the floating-point digital signal processor (DSP) from Texas Instrument (TI) (TMS320C6726) is adopted to implement the algorithm. The cyclone FPGA is used for the A/D sampling, protection, soft-start, and pulse width modulation (PWM) generation for the CHB-DSTATCOM.

The circuit parameters of the experimental set-up is the consistent with the digital simulation: L_g=100μH, R_g=50mΩ, L=2.0mH, r_L=50mΩ, and the dc-link circuit paramters are: $C_1=C_2=C_3$=2500μF, $R_1=R_2=R_3$=20kΩ, the sampling time T_s=100μs. The experimental results of the three module cascaded multilevel CHB-DSTATCOM are presented, and the obtained results are also discussed.

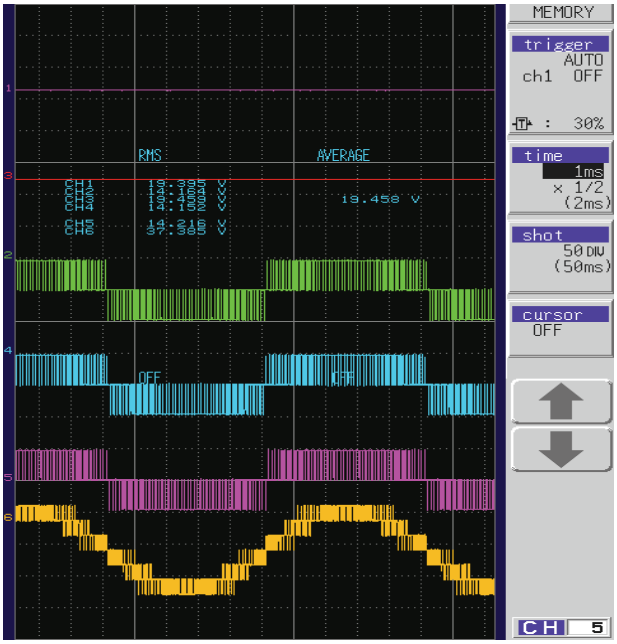


Fig.15 The synthesized 7-level voltage of the CHB-DSTATCOM.

Fig.15 shows the experimental results of the synthesized multilevel output voltage 'v_{aN}', and the dc-link voltages of the CHB-inverter at no load conditions. It can be observed that the dc-link voltages (ch-1, ch-3) are about 19.5V, and the output voltages of each inverter (ch-2, ch-4, ch-5) are about 14.2V, which are phase-shifted by 90 degrees in the PWM carriers. And the seven-level output voltage (ch-6) can also be observed in Fig.15.

Fig.16 shows the capacitve mode of the DSTATCOM. The RMS value of the dc-link voltages (ch-1, ch-2, ch-3) are about 20V and the waveforms show perfect matching with each other. The output waveform of the output voltage v_{a2} (ch-4) can also be observed. Besides, the grid current (ch-6) is leading the output multilevel voltage v_{aN} by 90 degrees, indicating that the CHB-DSTATCOM is injecting capacitive reactive power to the grid.

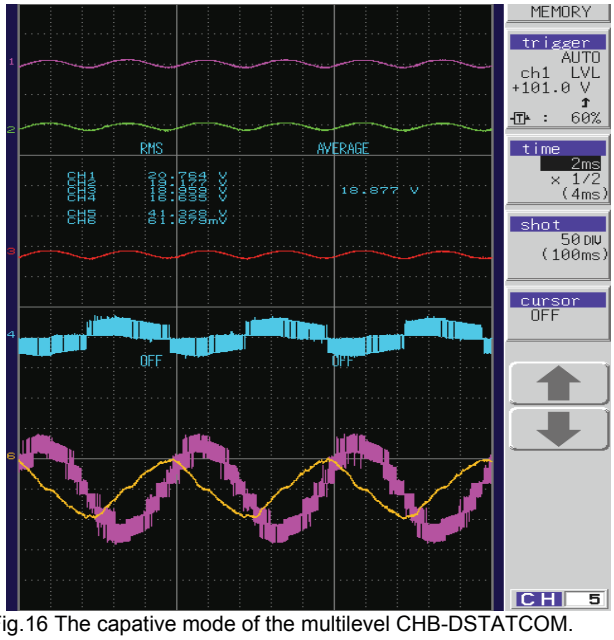


Fig.16 The capative mode of the multilevel CHB-DSTATCOM.

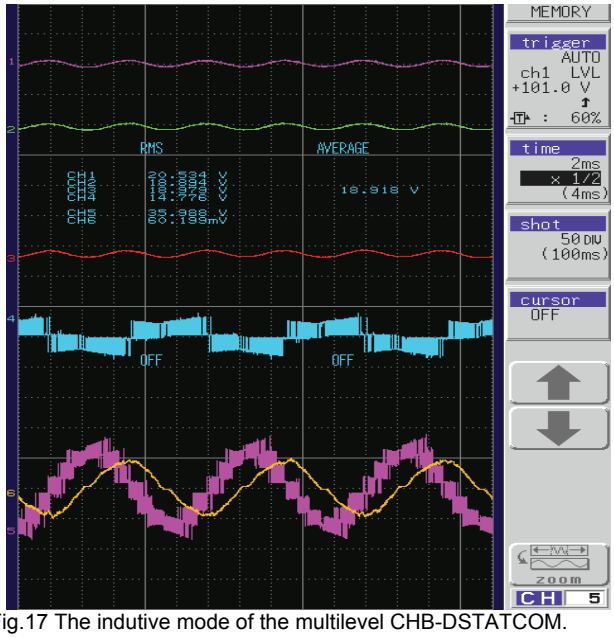


Fig.17 The indutive mode of the multilevel CHB-DSTATCOM.

Fig.17 shows the inductive mode of the DSTATCOM. The RMS value of the dc-link voltages (ch-1, ch-2, ch-3) are approximately 20V and the waveforms show perfect matching with each other. The output waveform of the output voltage v_{a2} (ch-4) can also be observed. Moreover, the grid current (ch-6) is lagging the output multilevel voltage v_{aN} by 90 degrees, indicating that the multilevel DSTATCOM is absorbing capacitive reactive power from the grid. It is interesting to notice that the waveforms recorded from the prototype system are consistent with the simulation results, which demonstrates the validity of the devised control algorithm.

Fig.18 shows the dynamic response of the multilevel DSTATCOM for reactive compensation of RL-type load. The dc-link voltages are denoted as 'ch-1,ch-2, ch-3', the synthesized multilevel output voltage is denoted as 'ch-5', the grid voltage is denoted as 'ch-4' and the grid current is denoted as 'ch-6'. Notably, the lower portion of Fig.18 is the enlarged view of the bracketed region in the upper portion. In Fig.18, the DSTATCOM is abruptly turned on and the dc-link voltage stabilization is achieved within half a fundamental cycle, and the grid current tracks the active component of the load current with excellent steady state precision and dynamic characteristics. Moreover, the grid current is in-phase with the grid voltage when the system is suddenly turned on.

From Figs.11-18, it can be concluded that the multilevel CHB-DSTATCOM is highly desirable for high voltage and high power applications due to the multilevel output voltage with reduced switching ripples and EMI noise. Besides, the devised passivity-based control algorithm is quite effective to ensure global stability of the CHB-DSTATCOM.

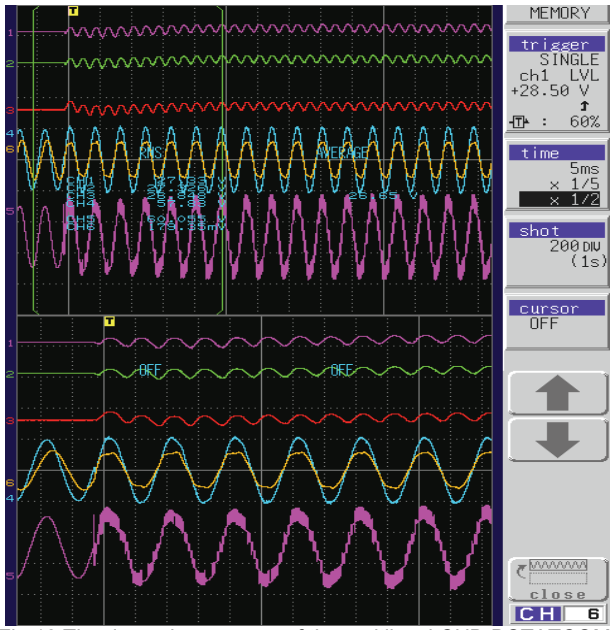


Fig.18 The dynamic response of the multilevel CHB-DSTATCOM.

VI. Conclusions and Future Work

This paper presents the passivity-based control scheme and the stable control region analysis for the cascaded H-bridge DSTATCOM. The mechanism of power balancing among the individual H-bridge modules are presented. Furthermore, the analysis of the stable control region (SCR) of the CHB-DSTATCOM is performed using the phasorial diagram representation with regard to the different dc-link voltages scenarios.

The simulation results obtained from the Alternative Transient Program - Electromagnetic Transient Program (ATP-EMTP) are presented for validation purposes. The effectiveness of the devised control algorithm is verified by the simulation results. Finally, the experimental results of the prototype system are presented, which reconfirms the validity and effectiveness of the control scheme.

The presented passivity-base control scheme can be extended to other grid-connected CHB-inverters, such as multilevel active rectifiers, active power filters, static series compensators (SSCs) for the renewable energy generation (such as wind power, solar), and power flow and power quality conditioning applications. The relevant results of these applications would be reported in the near future.

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