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Implementation of the Cascade Matrix Reactance Frequency Converter using Space Vector Modulation method

Abstract. *In this paper Cascade Matrix Reactance Frequency Converter (CMRFC) with direct space vector modulation and four step commutation strategy is analyzed. Presented direct AC/AC converter allows to create output voltages with desired frequency and buck- boost voltage transfer ratio, furthermore input power factor improvement is possible. Description of CMRFC structure and control is presented. In order to confirm its features some simulation and experimental results are presented.*

Streszczenie. *Przedmiotem artykułu jest układ kaskadowego matrycowo- reaktancyjnego przemiennika częstotliwości (KMRPC) o bezpośredniej modulacji wektorowej i czterostopniowej strategii komutacji. Prezentowany bezpośredni przekształtnik AC/AC pozwala na uzyskanie napięcia wyjściowego o zadanej częstotliwości oraz wzmocnieniu napięiowym typu buck- boost dodatkowo poprawa wejściowego współczynnika mocy jest możliwa. W artykule przedstawiono opis topologii oraz sterowania KMRPC. W celu potwierdzenia właściwości układu zaprezentowano wyniki badań symulacyjnych i eksperymantalnych (**Implementacja Kaskadowego Matrycowo- Reaktancyjnego Przemiennika Częstotliwości o modulacji wektorowej**)*

Keywords: AC/AC frequency converters, matrix converter, space vector modulation method.
Słowa kluczowe: przekształtniki AC/AC, przekształtniki matrycowe, modylacja wektorowa.

Introduction

The AC/AC frequency converters without large DC storage elements are the most probable successors for commonly used pulse width modulated (PWM) back to back (B2B) converters (PWM rectifier and PWM inverter) [1]-[14]. Voltage Source Matrix Converter (VSMC), a well-known competitor for B2B converter is smaller then B2B and has longer life period, because of the lack of the bulky DC storage link. However VSMC comparing to B2B converter has poor voltage transfer ratio (q) which is defined as ratio between the output and input voltage. VSMC voltage transfer ratio cannot be higher than 0.866 [1]-[4] if input and output waveforms should be sinusoidal. This disadvantage strongly reduce amount of possible VSMC applications.

In the recent years couple solutions have been considered to overcome this VSMC disadvantage. The easiest way to increase VSMC q is to connect it to the grid via the transformer. However such converter will be bulky because of the transformer size for the grid frequency.

In Ref. [5] VSMC with fictitious DC link vector modulation is presented. With this modulation VSMC q up to 1.053 is achieved at the expense of low frequency distortion in the input and output waves.

Another interesting solution for the low VSMC q is Current Source Matrix Converter (CSMC) [6], [10]. With this direct AC/AC converter, by a proper control of the output current, output voltages with desired frequency and amplitude grader then one are generated. Furthermore correction of the input power factor is possible. However the problem is, that there are no natural current sources so extra inductivities in series connection with voltage sources are necessarily. Because CSMC is a current converter it's voltage transfer ratio depends on load.

In Ref. [7] the concept of the Hybrid Matrix Converters is presented. In this solution Indirect Matrix Converter (IMC) (AC/DC/AC converter without DC storage elements which has similar features to the VSMC) is used. To mitigate IMC low q a boost converter is added to the DC link of the IMC, so the cost of the boost functionality is an extra capacitance and four extra semiconductors.

Other interesting AC/AC frequency converters solution, with which both frequency change and the buck-boost load voltage conversion is possible are the Integrated Matrix Reactance Frequency Converters (IMRFC) [8], [9], [11]. IMRFC are built of VSMC or CSMC with additional passive elements and three synchronous switches connected on load or source side during the control of the MRFC, MC part must be synchronized with synchronous switches.

Recently a new solution of the Cascade Matrix Reactance Frequency Converter (CMRFC) was presented [12]. This topology consists of Boost Matrix Reactance Chopper (BMRC) with reduced number of switches which is connected the input side of the Matrix Converter. Comparing IMRFC with CMRFC, for the second one five additional transistors are required but no extra passive elements are needed since VSMC input filter reactance is used as a boost reactance for BMRC. Furthermore there is no need to synchronize VSMC part of the CMRFC with its BMRC part.

In this paper Cascade Matrix Reactance Frequency Converter with direct space vector control strategy is analyzed. Authors in Ref. [12] are focused on work description and filter design for CMRFC with implemented so called Indirect Vector Control Strategy. It seems that deeper studies of the IMRFC features are needed. Lack of those studies does not allow for a comparison of the Cascade Matrix Reactance Converter with other converters especially with Integrated Matrix Reactance Frequency Converters. Furthermore there are no simulation or experimental results for CMRFC with direct vector modulation for which no factious DC link is needed. That is why those simulation and experimental studies are delivered in this article.

The next section contains the description of the Cascade Matrix Reactance Frequency Converter topology. Control is described in Section 3. In Section 4 simulation and experimental results are shown. Conclusions follow in the last section.

Converter description

The basic scheme of the three-phase Cascade Matrix Reactance Frequency Converter is shown in Fig. 1. This converter consists of 13 bidirectional switches. It is built of Boost Matrix Reactance Chopper (BMRC) with reduced number of switches (4 bidirectional switches) and Matrix Converter (nine bidirectional switches) [12].

In this converter BMRC part is responsible for voltage gain whereas MC part for frequency change and power factor control. Ideal input-output voltage relationships for BMRC can be expressed by (1) [13]. Matrix Converter input- output voltage relationships are expressed by (2) [1].

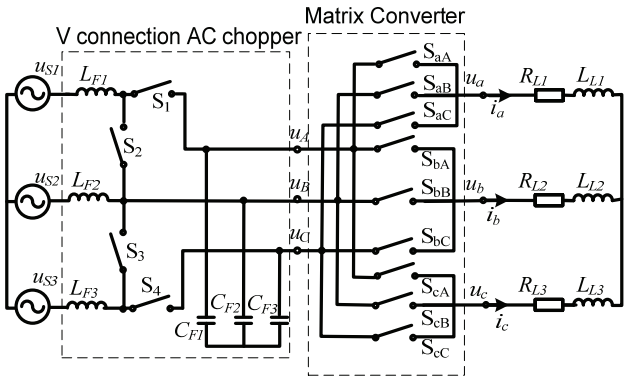

Fig. 1 Topology of the Cascade Matrix Reactance Frequency Converter

$$\begin{bmatrix} u_A \\ u_B \\ u_C \end{bmatrix} \approx \begin{bmatrix} \frac{1}{1-D} & 0 & 0 \\ 0 & \frac{1}{1-D} & 0 \\ 0 & 0 & \frac{1}{1-D} \end{bmatrix} \begin{bmatrix} u_{S1} \\ u_{S2} \\ u_{S3} \end{bmatrix} \quad (1)$$

where *D*- duty cycle for chopper switches

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \begin{bmatrix} s_{aA} & s_{aB} & s_{aC} \\ s_{bA} & s_{bB} & s_{bC} \\ s_{cA} & s_{cB} & s_{cC} \end{bmatrix} \begin{bmatrix} u_A \\ u_B \\ u_C \end{bmatrix} \quad (2)$$

where: s_{jK} – state function of the switch S_{jK}.

Presented converter can be built almost as compact as original Voltage Source Matrix Converter. Because of the switching frequency which is much higher than the power grid frequency input capacitors and inductivities are the same size as for Matrix Converter filter. So only additional components are four bidirectional switches. Furthermore CMRFC does not required any voltage control in the input capacitor since on both input and output sides of the Boost Matrix Reactance Chopper are AC voltages [9]. Because of commutation laws, for a Matrix Converter there are only 27 switching configurations (SCs) permitted among witch 21 SCs (18 active, 3 zero) (Fig. 2), are engaged in direct space vector control DSVC which will be described in the next section.

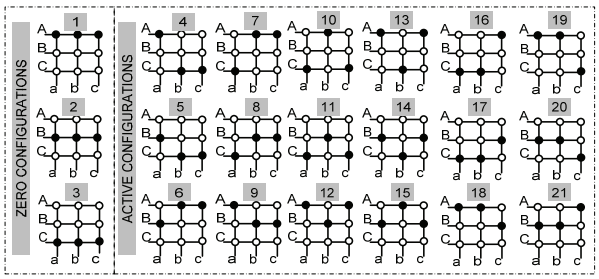

Fig. 2 Geometrical representation of the 21 switch configurations engaged in direct space vector control

Control description

Cascade Matrix Reactance Frequency Converter is a connection of two well-known converters: Boost Matrix Reactance Chopper and a Matrix Converter. In CMRFC those two converters do not need to be synchronized with each other and both are controlled separate.

In Fig. 3 basic diagram of the control sequence with task division for hardware in which it is implemented, is shown. Control hardware basically consists of two ADSP21836 DSP processors, one XC3S200 FPGA circuit and three A/D converters.

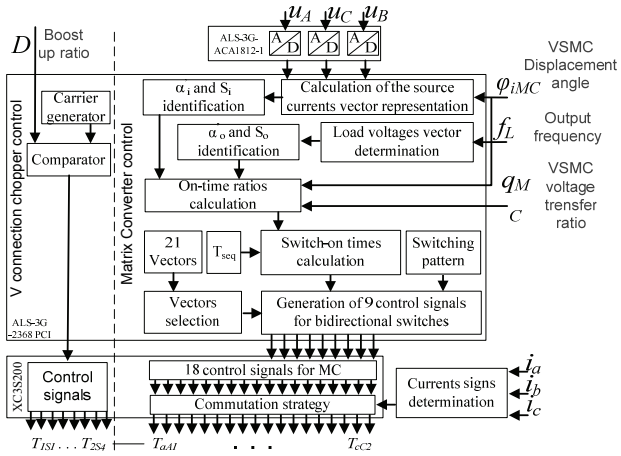

Fig. 3 Control sequence diagram Cascade Matrix Reactance Converter

If a required voltage transfer ratio (q) is less than 0.866 BMRC can be neglected by switching on switches S_1, S_4 and off S_2, S_3. In this state both voltage and frequency transformation is realized by VSMC part. If output voltage greater than 0.866 is needed, BMRC provides on the input side of the VSMC boosted up source voltages, which frequency can be changed by VSMC. Furthermore input power factor correction can be achieved by proper control of the VSMC part.

Boost Matrix Reactance Converter is controlled with a standard PWM algorithm where carrier waveform is compared with a boost up ratio D. According to desired duty cycle bidirectional switches S_2 and S_3 are closed whereas S_1 and S_4 are open, at this time energy is accumulated in input inductivities. In the next step when S_2 and S_3 are open and S_1 and S_4 are closed accumulated energy is transmitted to the Matrix Converter which works non-stop during the whole described process (Fig. 3, 5). BMRC and VSMC are working independently so VSMC can realize any of well-known control strategies. In this article a direct vector control strategy DVCS for VSMC was implemented.

Implemented DVCS is based on instantaneous vector representations for, 21 SCs (Fig. 2), of the input, output voltages and currents (Fig. 4) [3], [14].

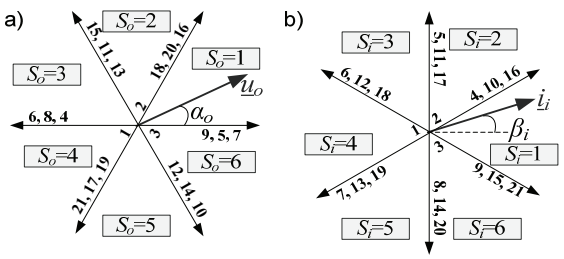

Fig. 4 Space vector representations for, (a) load line to neutral voltages (u_{aN}, u_{bN}, u_{cN}), (b) input line currents $u_o=e^{j\alpha_o}$ is an exemplary the vector position of line to neutral load voltages, $i_i=e^{j\beta_i}$ stands for an exemplary vector position of line source currents, S_o means the sector number for $\underline{u}_0$, S_i denotes the sector number for $\underline{i}_j$

By Direct Space Vector Control (DSVC) first of all position of the output voltages vector $\underline{v}_o$, which represents instantaneous values of the CMRFC output voltages, is set. This position is described by sector number S_o, in which $\underline{v}_o$ is currently placed, and phase angle α'_o (Figs. 4(a) and 6(a)).

In the next step position of the VSMC input currents vector $\underline{i}_i$, with respect to the desired displacement angle φ_{iMC}, is found and defined by sector S_i and angle β'_i (Figs. 4(b) and 6(b)). Found $\underline{i}_i$ vector represents instantaneous values of the VSMC input currents. Angles α'_o and β'_i are defined with respect to the bisecting line of the suitable sectors. Based on collected data on-time ratios are calculated according to (3)-(6). In the last step four active switching configurations (vectors) are selected according to table 1.

$$\delta_1 = (-1)^{S_0+S_i+1}\frac{2}{\sqrt{3}}q\frac{\cos(\alpha'_0-\pi/3)\cos(\beta'_i-\pi/3)}{\cos\varphi_{iMC}} \quad (3)$$

$$\delta_2 = (-1)^{S_0+S_i}\frac{2}{\sqrt{3}}q\frac{\cos(\alpha'_0-\pi/3)\cos(\beta'_i+\pi/3)}{\cos\varphi_{iMC}} \quad (4)$$

$$\delta_3 = (-1)^{S_0+S_i}\frac{2}{\sqrt{3}}q\frac{\cos(\alpha'_0+\pi/3)\cos(\beta'_i-\pi/3)}{\cos\varphi_{iMC}} \quad (5)$$

$$\delta_4 = (-1)^{S_0+S_i+1}\frac{2}{\sqrt{3}}q\frac{\cos(\alpha'_0+\pi/3)\cos(\beta'_i+\pi/3)}{\cos\varphi_{iMC}} \quad (6)$$

$$t_1 = |\delta_1|T_{seq};\ t_2 = |\delta_2|T_{seq};\ t_3 = |\delta_3|T_{seq};\ t_4 = |\delta_4|T_{seq} \quad (7)$$

Table 1 Summary of the active switching configurations (vectors) assigned to the sectors S_o i S_i and on time rations δ_1 -δ_4

	SC δ_1		SC δ_2		SC δ_3		SC δ_4	
(S_i = 1∨4) ∧ (S_o=1∨4)	*19*	*16*	*21*	*18*	*7*	*4*	*9*	*6*
(S_i = 2∨5) ∧ (S_o=1∨4)	*17*	*20*	*19*	*16*	*5*	*8*	*7*	*4*
(S_i = 3∨6) ∧ (S_o=1∨4)	*21*	*18*	*17*	*20*	*9*	*6*	*5*	*8*
(S_i = 1∨4) ∧ (S_o=2∨5)	*13*	*10*	*15*	*12*	*19*	*16*	*21*	*18*
(S_i = 2∨5) ∧ (S_o=2∨5)	*11*	*14*	*13*	*10*	*17*	*20*	*19*	*16*
(S_i = 3∨6) ∧ (S_o=2∨5)	*15*	*12*	*11*	*14*	*21*	*18*	*17*	*20*
(S_i = 1∨4) ∧ (S_o=3∨6)	*7*	*4*	*9*	*6*	*13*	*10*	*15*	*12*
(S_i = 2∨5) ∧ (S_o=3∨6)	*5*	*8*	*7*	*4*	*11*	*14*	*13*	*10*
(S_i = 3∨6) ∧ (S_o=3∨6)	*9*	*6*	*5*	*8*	*15*	*12*	*11*	*14*
	$\delta_1>0$	$\delta_1<0$	$\delta_2>0$	$\delta_2<0$	$\delta_3>0$	$\delta_3<0$	$\delta_4>0$	$\delta_4<0$

By switching on four selected switching configurations, for a proper time (7) during the switching time period T_{sequ} (Fig. 5), input currents and output voltages are created (Fig. 6). Switching time period should be completed by switching on one zero vectors selected with respect to the smallest commutation number.

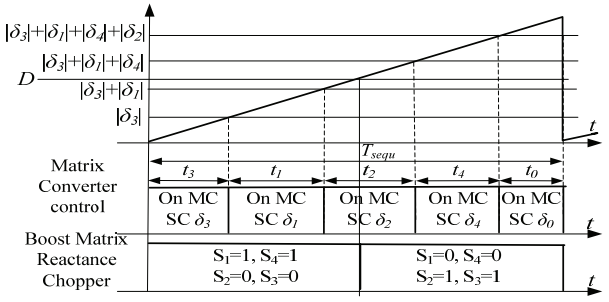

Fig. 5 Calculation of the duty cycles for Voltage Source Matrix Converter (VSMC) switching configurations (SCs) and Boost Matrix Reactance Chopper (BMRC) switches

In Fig. 6 it is shown how example vector $\underline{u}_o$, which represents instantaneous values of the CMRFC load phase voltages, and vector $\underline{i}_i$, which represents instantiates values of the VSMC input phase currents, are synthesized. Output voltage vector $\underline{u}_o$ is set up of two components $\underline{u}'_o$ and $\underline{u}''_o$ (Fig 6(a)). Vector $\underline{u}'_o$ is created by switching on vector 21 for the time t_2 and vector 16 for the time t_1, vector $\underline{u}''_o$ is set up by switching on vector 7 for the time t_3 and vector 6 for the time t_4. Vector $\underline{i}_i$ is synthesized analogical to $\underline{u}_o$ (Fig. 6(b)), furthermore on Fig. 6(b) it is shown how the control of displacement angle between VSMC input currents and voltages φ_{iMC} is achieved.

To avoid short circuits and over voltages during the commutation process for VSMC part a four step commutation strategy described in Ref. [4] was implemented. The BMRC part is protected by overvoltage clamp circuit.

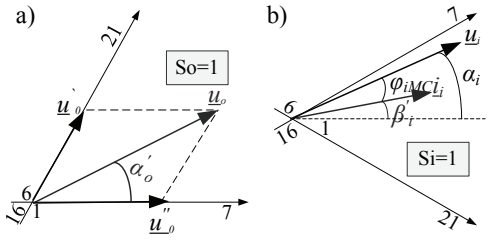

Fig. 6 Vector modulation principle: (a) for exemplary output voltage vector position, (b) for exemplary input current vector position

Simulation and experimental results

In this section selected simulation and experimental test results are presented. For the simulation analysis, the software of Matlab Simulink is used. In order to confirm simulation tests results 1kVA Cascade Matrix Reactance Frequency Converter including control setup was built [15]. Simplified scheme and photo of the laboratory implementation is shown in Fig. 7. Simulation and experimental circuit's parameters are collected in Table 2.

Table 2. Parameters of the simulation and experimental circuits

Parameter	Symbol	Value	
Source voltages amplitude and frequency	U_s / f	Simulation	Experiment
		230 V/50 Hz	40 V / 50 Hz
Switching time period	T_{sequ}	0.1 ms	
Inductance	L_F	1.5 mH	
Capacitance	C_F	10 μF	
Resistance	R_L	30 Ω	

Simulation and experimental tests results are collected in Figs. 8-14. Implemented converter without DC storage link makes it possible to set output voltage amplitude higher than input voltage amplitude. In Fig. 8(a) input voltage (u_{s1}), input current (i_A), output voltage (u_a) and filtered output voltage (u_{aLPF}) time waveforms for D set to 0.6 and q_{MC} set to 0.866 are shown. Experimental time waveforms for the same parameters are shown in Fig. 8(b). In both simulation and experimental results voltage transfer ratio is near 2.

In presented converter both output voltage amplitude and frequency can be set independently. In Fig. 9 simulation time waveforms with desired output voltage first harmonic frequency 25 Hz, 50 Hz 75 Hz, are shown. The same experimental time waveforms are shown in Fig. 10.

Using CMRFC with Space Vector Control, some adjustments of the displacement angle φ_i between input voltages and currents (by setting up φ_{iMC}) are possible. In Fig. 11 simulation and in Fig. 12 experimental time waveforms of the CMRFC with desired displacement between VSMC input current and voltage (φ_{iMC}) are shown. In Fig. 13(a) voltage transfer ratio (u_s/u_o) as a function of D is shown. However this characteristic contains only a boost part of the CMRFC characteristic, it means that VSMC transfer ratio q_{MC} is constantly set to 0.866 value. If CMRFC voltage transfer ratio lower than 0.866 is need both S1 and S2 switches are closed then CMRFC works as a normal Voltage Source Matrix Converter with a voltage transfer ratio from 0 to 0.866.

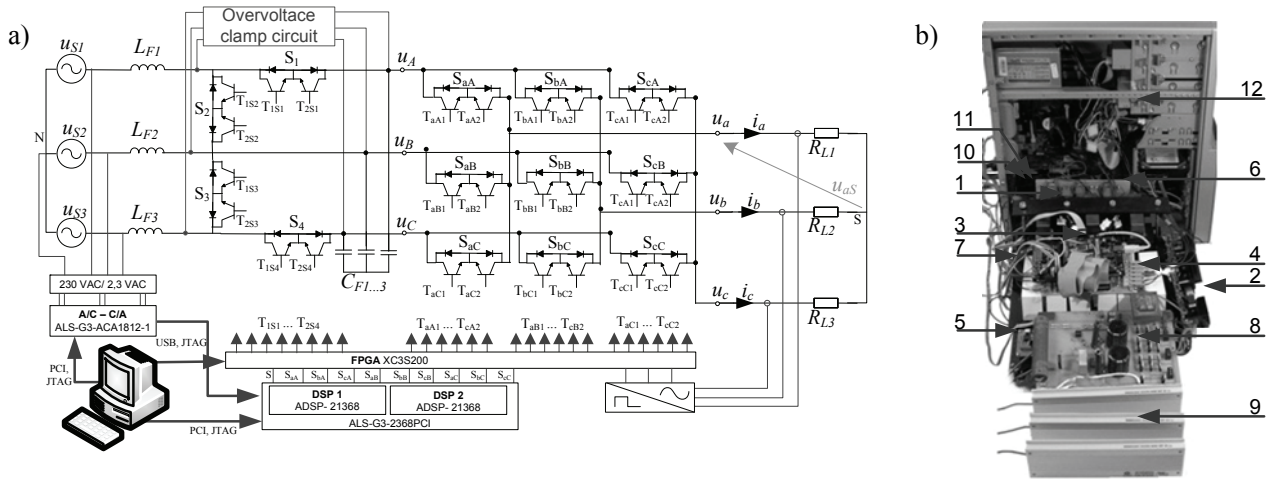

Fig. 7 Cascade Matrix Reactance Converter (a) simplified schema, (b) prototype 1– input filter; 2– AC adapter; 3– FPGA board; 4– optical transmitters; 5– load current measurement circuit; 6- source voltage measurement circuit; 7– optical receivers and transistor drivers; 8– protection clamp circuit; 9– load resistance; 10–DSP board (ALS-G3-2368PCI) 11– A/D converters (ALS-G3-ACA1812-1); 12- PC

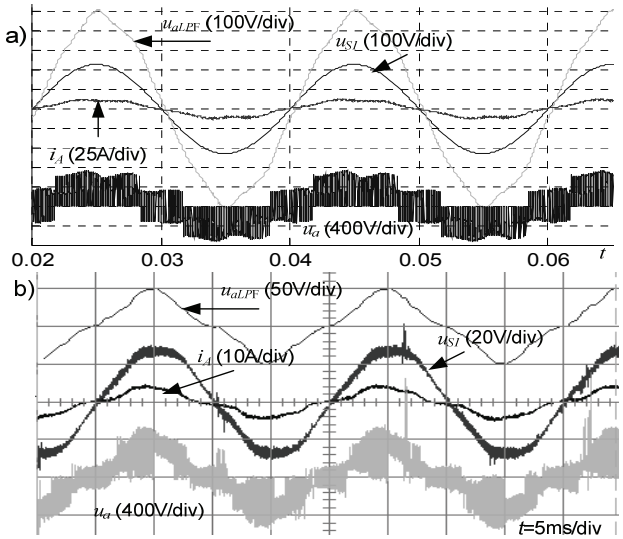

Fig. 8 Time waveforms for D=0.6 and q_{MC}=0.866 , (a) simulation, (b) experiment. i_A- source current, u_{s1}- source voltage, u_a- load voltage, u_{aLPF}- filtered load voltage

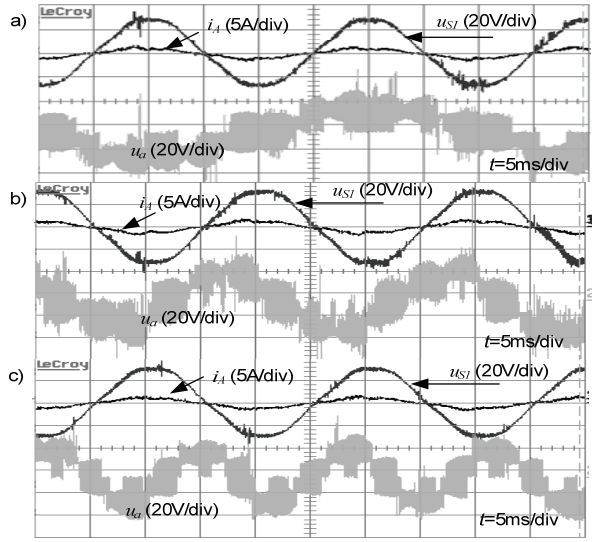

Fig. 10 Experimental time waveforms of the source current (i_A), source voltage (u_{s1}) and load voltage (u_a) with desired frequency (a) 25 Hz, (b) 50 Hz, (c) 75 Hz

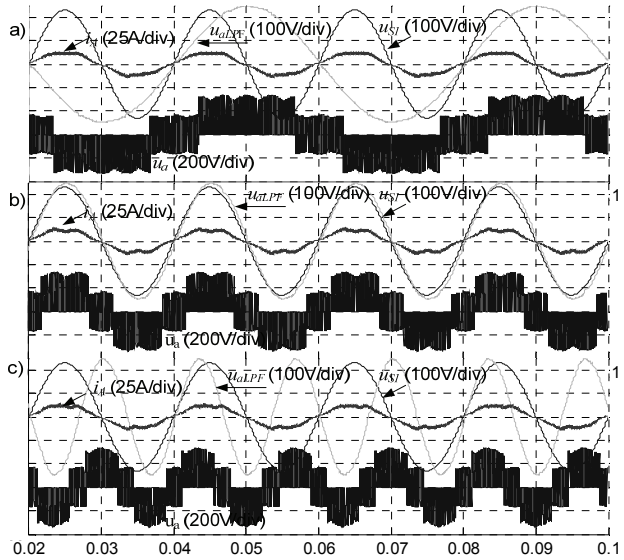

Fig. 9 Simulation time waveforms of the source current (i_A), source voltage (u_{s1}), load voltage (u_a) and filtered load voltage (u_{aLPF}) with desired frequency (a) 25 Hz, (b) 50 Hz, (c) 75 Hz

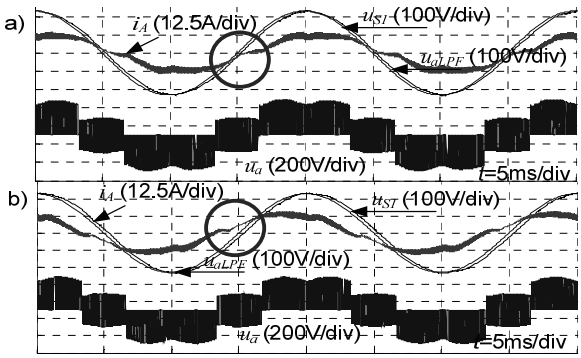

Fig. 11 Simulation time waveforms for D=0.7, q_{MC}=0.7, f_L=50 Hz and (a) φ_{iMC}=0.5, (b) φ_{iMC}=-0.5

In Fig. 13(b) input power factor changes as a function of D are shown. However it is possible to correct this input power factor by a proper adjustment of the VSMC displacement angle φ_{iMC}.

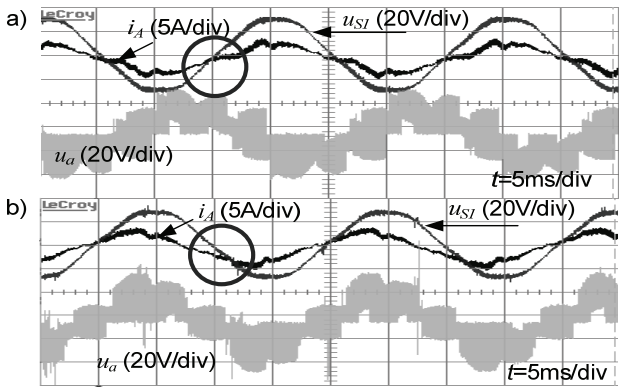

Fig. 12 Simulation time waveforms for D=0.7, q=0.7, fL=50 Hz and (a) φ_{iMC}= 0.5 rad, (b) φ_{iMC}= -0.5 rad

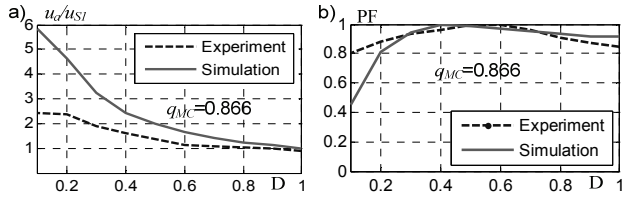

Fig. 13 (a) Output/input voltage ratio (u_s/u_o) as a function of D by q=0.866, (b) Input power factor (PF) as a function of D by q=0.866

In CMRFC voltage transfer ratio can by controlled by setting up two components D (BMRC boost up ration) and q_{MC} (VSMC voltage transfer ratio), input power factor can be adjusted by setting up VSMC φ_{iMC} parameter. If φ_{iMC} (power factor) is changed it needs to be noted that:

$$q_{MC\_MAX} = 0.866 \cdot \cos(\varphi_{iMC}) \tag{8}$$

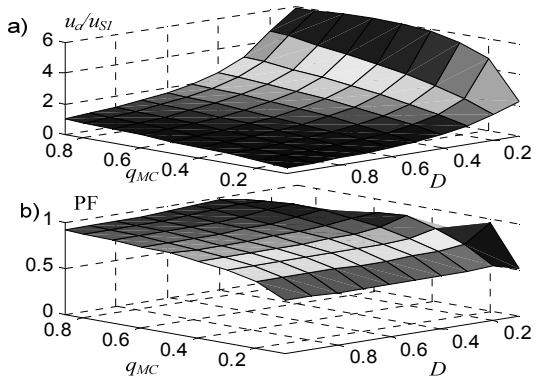

Fig. 14 Simulation test (a) CMRFC voltage transfer ratio, (b) CMRFC input power factor for all possible combinations of q_{MC} and D.

In Fig. 14(a) simulation CMRFC voltage transfer (u_a/u_{SI}) and in Fig 14(b) input power factor (PF) for all possible combinations of q_{MC} and D parameters are shown.

Conclusions

In this article Cascade Matrix Reactance Frequency Converter witch direct space vector control was presented. Both simulation and experimental tests confirmed that this direct AC/AC converter allows to change input voltage frequency and to set voltage transfer ratio from zero up to much more than one. It was also confirmed that power factor correction is possible. Future work will be focused on comparing presented cascade matrix reactance converter with integrated one. Furthermore the cause of current disturbance must be found.

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