Jianping HU, Qi CHEN
Ningbo University

Modelling and Near-Threshold Computing of Power-Gating Adiabatic Logic Circuits

Abstract. *This paper introduces a power-gating scheme appropriate for near-threshold operating of single-phase adiabatic circuits. A transmission gate with MOS bootstrapping scheme is used as the power-gating switch, which is used to reduce energy overhead. CAL (Clocked Adiabatic Logic) circuits are investigated. The analytical model for power-gating adiabatic circuits is constructed, and the energy overhead of the proposed power-gating scheme is analyzed in detail. The results show that the proposed power-gating technique is suitable for near-threshold operating.*

Streszczenie. *W artykule wprowadzono schemat bramkowania mocy dla progowej operacji jednofazowych obwodów adiabatycznych. Zaproponowano model analityczny bazujący na układach MOS jako przełącznikach bramkujących. (**Modelowanie i obliczanie stanów progowych bramkowania mocy w adiabatycznych obwodach logicznych**)*

Keywords: Near-Threshold Computing; Modeling; MOS Bootstrapping, Single-Phase Energy-Recycling Circuits.
Słowa kluczowe: adiabatyczne obwody logiczne, bramkowanie mocy.

Introduction

As CMOS devices approach nanometer processes, power consumption has become a critical concern [1]. The energy consumption in integrated circuits has mainly two components: switching energy and static energy. The total energy consumption per cycle can be written as [2]

$$E_{\text{total}} = E_{\text{dyn}} + E_{\text{leakage}} = C_{\text{L}} {V_{\text{DD}}}^2 + V_{\text{DD}} I_{\text{leakage}} T \tag{1}$$

where C_L is the load capacitance, V_{DD} is source voltage, T is operation cycle, and $I_{leakage}$ is leakage current, respectively. A direct solution for reducing energy is to scale down supply voltage, since switching energy is reduced quadratically and leakage decreases linearly as supply voltage scales down [3]. Sub-threshold circuits can reach minimum energy but only suits for ultra-low performances [4]. In order to attain more extensive application, scaling supply voltage to near-threshold region is an attractive approach for mid performances [5].

Adiabatic logic utilizes AC power-clock to recover effectively the charge delivered by the clock instead of being dissipated to the ground [6-8]. In order to reduce the energy dissipation of the adiabatic circuits in sleep mode, power-gating schemes for adiabatic circuits have been also introduced [9]. However, the previously power-gating adiabatic logic circuits focus mainly on nominal voltage circuits. To the best of our knowledge, no previous investigates for near-threshold power-gating adiabatic circuits are presented.

This paper is organized as follows. In section 2, CAL (Clocked Adiabatic Logic) circuits are reviewed. In section 3, the power-gating scheme for single-phase adiabatic circuits that is appropriate for near-threshold operating is introduced. The analytical model for power-gating adiabatic circuits and the detailed analysis for energy overhead of the proposed power-gating scheme are also given in section 4. The experimental results of the power-gating scheme proposed in this paper with an 8-bit full adder are presented in section 5. Finally, our work of this paper is summarized in the last section.

Improved CAL circuits

The CAL buffer is shown in Fig. 1(a) [7]. The logic evaluation circuit consists of the two NMOS transistors (N1, N2). *CX* is an auxiliary clock signal, and it enables the evaluation NMOS transistors (N1, N2) by turning on the NMOS transistors (N5, N6). The energy recovery circuit consists of the two cross-coupled PMOS transistors (P1, P2). The power-clock *clk* charges the output (*OUT* or *OUTb*) in evaluation phase through P1 and P2. In recovery phase, the energy of the output nodes is recovered to *clk* through P1 and P2. The clamp transistors (N3 and N4) ensure stable operation by preventing from floating of the output nodes.

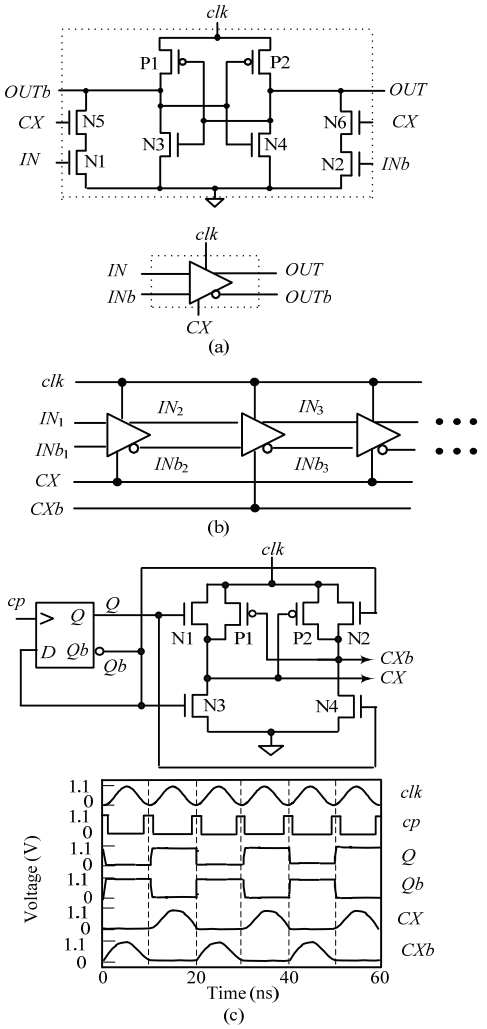

Fig.1. Improved CAL buffer. (a) schematic, and (b) symbol and buffer chain, and (c) auxiliary clock generator and its simulation waveforms

The cascaded CAL circuits are supplied by a single-phase power clock, as shown in Fig. 1(b). The two-phase non-overlap sinusoidal clocks (*CX* and *CXb*) are used for the auxiliary lines instead of the square wave clocks, as shown in Fig. 1(c). They are generated with an auxiliary clock generator. The operation waveforms of the auxiliary clock generator are also shown in Fig. 1(c).

Power-gating scheme for near-threshold computing

The proposed power-gating scheme for near-threshold CAL circuits is shown in Fig. 2. A transmission gate (N_{PGS} and P_{PGS}) along with a NMOS transistor (NC) is used as the power-gating switch (PGS), which is inserted between the single-phase power-clock (*pc*) and virtual power-clock (*clk*). A clamp NMOS transistor (NC) prevents the floating state of the virtual power-clock in sleep mode. The power-gating switch (PGS) is switched by the power-gating control circuit (PGCC) that consists of the two static CMOS inverters and a NMOS transistor (NB). During active periods, the node active can be bootstrapped to provide full swing operation and reduce the turn-on resistance.

The simulated waveforms of the power-gating scheme for the single-phase adiabatic circuits are shown in Fig. 3. The frequency of the power-clocks was 100MHz, and its peak-to-peak voltage (V_{DD}) was taken with 1.1V. The device size of the bootstrapping NMOS switch N_{PGS} is taken with 60*λ*/2*λ* (*λ*=23nm). The device size of the PMOS transistor N_{PGS} and the power-gating control transistor NB are all taken with 3*λ*/2*λ*, since they only are supplementary for bootstrapping NMOS switch N_{PGS}. For static CMOS inverters, the device size of NMOS and PMOS transistors was taken with 3*λ*/2λ and 6λ/2λ, respectively.

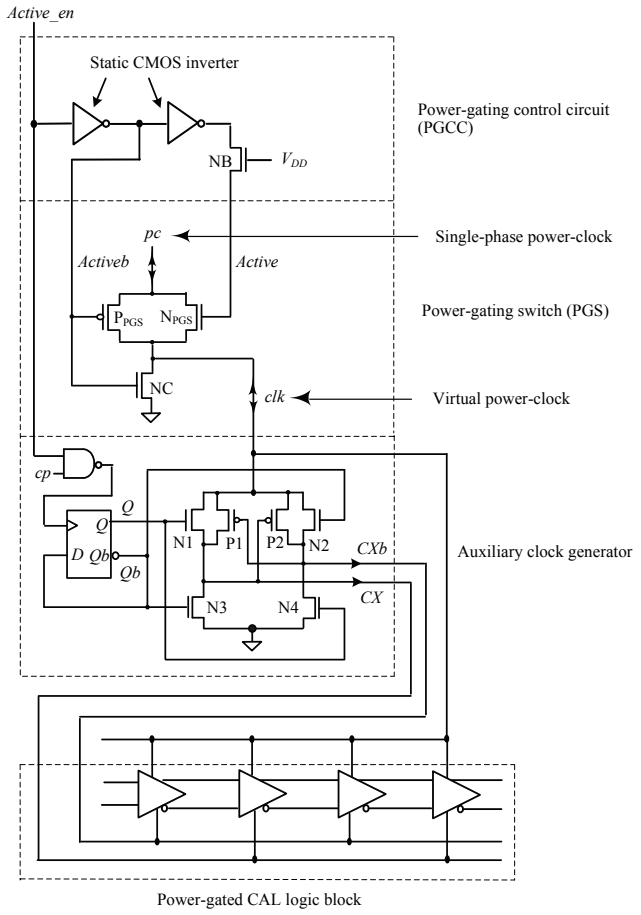

Fig.2. Power-gating scheme for near-threshold single-phase CAL circuits

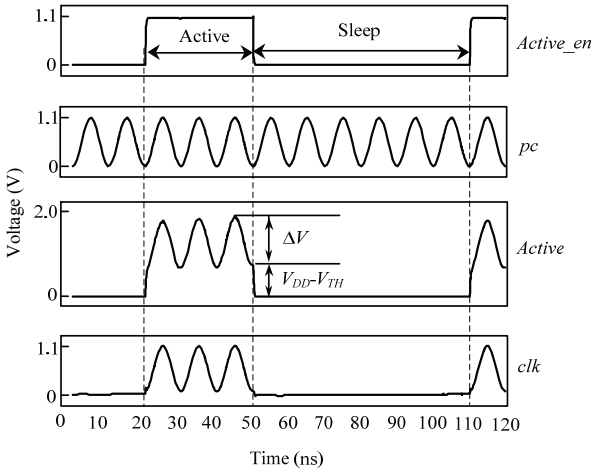

Fig.3. Simulation waveforms of power-gating scheme for near-threshold single-phase CAL circuits

In the active mode, the active input signal *active_en* is set to V_{DD}, so that the node *activeb* is clamped to ground, and the node *active* is charged to about $V_{DD} - V_{TN}$, where V_{TN} is the threshold voltage of the NMOS transistor. Therefore, in active mode, the power-gating NMOS N_{PGS} and PMOS P_{PGS} are turned on. The virtual power-clock *clk* follows the power-clock *pc* to power the adiabatic logic block.

As shown Fig. 3, in the active mode the voltage of the node *active* can be bootstrapped to a higher level than $V_{DD} - V_{TN}$ due to the gate-to-channel capacitance of the transistor N_{PGS} while *pc* is varying. As the clock *pc* rises from 0V to V_{DD}, the voltage increment of the bootstrapped node *active* is determined by the following expression

$$\Delta V = \frac{V_{DD} C_G}{C_D} + C_G \tag{2}$$

where $C_G = WLC_{OX}$ is the gate-to-channel capacitance of N_{PGS}, *W* and *L* are the channel width and length of N_{PGS}, C_{OX} is the gate-to-channel capacitance per unit area, and C_D is the diffusion capacitance of the NB, respectively. In order to obtain a good operation for the power-gated adiabatic logic blocks, the bootstrapped voltage of the node *active* should be high enough to turn on the power-gating NMOS switch N_{PGS}.

Modeling and analysis for energy overhead of powrer-gating scheme

Here we consider the power-gating logic block with the power-gating switches (Fig. 2) and the no-power-gating logic block without the power-gating switches. In the no-power-gating logic block, all logic circuits are directly connected to power-clocks (*pc*), and the entire logic block is powered at all times.

For power-clocks, the adiabatic logic block can be modeled by an equivalent capacitor C_{ALB}, in series with a resistor R_{ALB}, as shown in Fig. 4 (a), which model energy storage and the energy loss of the logic block, respectively. The model parameters of power-gated adiabatic logic block are given by

$$R_{ALB} = \frac{E_{\mathrm{ALB}} f}{I^2} \tag{3}$$

$$C_{ALB} = \frac{\sqrt{2} I}{\pi V_{DD}} f \tag{4}$$

where E_{ALB} is the energy loss per cycle of the power-clock *clk*, *I* is the rms current through R_{ALB}, and *f* and V_{DD} are the frequency and the peak-to-peak voltage of the power-clock, respectively.

For the logic block with power-gating switches, the power-gating switch PGS is turned on during whole active periods. Fig. 4(a) shows the equivalent circuit of the logic block and power-gating switch in the active mode. The RPGS is inserted, which consists mostly of turn-on resistance of N_{PGS}, since the PMOS transistor P_{PGS} only uses small device size.

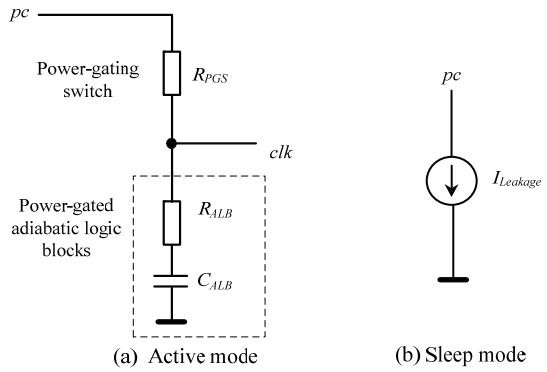

Fig.4. Equivalent circuit of adiabatic logic block and power-gating switches

According to (2), $\Delta V \approx V_{DD}$, since the size of the transistor N_{PGS} is much larger than transistor NB. Therefore, the gate-to-source voltage of N_{PGS} is almost a constant, V_{DD}–V_{TN}. The turn-on resistance of PGS can be approximately written as

$$R_{PGS} = \frac{1}{\mu C_{OX} \frac{W}{L}(V_{DD} - V_{TN})} \tag{5}$$

where μ is the carrier mobility, and W and L are the channel width and length of N_{PGS}, respectively.

In the sleep mode, the power-gating switch is turned off, so that the power-clock are detached from the adiabatic logic block. Fig. 4(b) shows the equivalent circuit of the power-gating switch in the sleep mode, where $I_{leakage}$ is its average leakage current, which should be take into account because of large transistor sizes.

In the active mode, the node *active* is bootstrapped, and the transistor NB is isolated, thus energy loss on the node *active* can be ignored. Therefore, the energy loss per cycle introduced by power-gating switch can be written

$$E_{PGS} = (\frac{\pi^2}{2})(\frac{R_{PGS} C_{\mathrm{ALB}}}{T}) C_{\mathrm{ALB}} {V_{\mathrm{DD}}}^2 \tag{6}$$

Energy dissipation of the power-gating adiabatic circuits in active mode are given by

$$E_{active} = E_{ALB} + E_{PGS} \tag{7}$$

The energy overhead of the power-gating switches in active mode is defined as the ratio of the dissipated energy in the power-gating switches and the adiabatic logic block

$$\eta_{PGS} = \frac{E_{PGS}}{E_{ALB}} = \frac{R_{PGS}}{R_{ALB}} \propto \frac{1}{W/L} \tag{8}$$

From (8), the energy overhead is in inverse proportion to the channel width of the N_{PGS}. By increasing the channel width, the energy overhead can be reduced.

The energy loss of the power-gating switches is caused by the leakage current $I_{leakage}$ of the power-gating transistor N_{PGS} because of large transistor sizes, which is represented as

$$E_{\mathrm{sleep}} = \frac{I_{\mathrm{leakage}} V_{DD}}{2} \tag{9}$$

The leakage energy loss Eleakage is mostly proportional to the channel width of the power-gating transistor N_{PGS}.

Additional energy is needed to turn-on and turn-off the gating switch. In order to turn-on the power-gating NMOS switch N_{PGS}, the node active is charged from 0V to V_{DD} – V_{TH}, while the node *activeb* is clamped from V_{DD} to 0V. During the next sleep period, the nodes *active* is discharged to 0V, and the node *activeb* is charged from 0V to V_{DD}. Therefore, energy loss per switching for each power-gating switch can be written as

$$E_{switch} = C_{activeb} {V_{\mathrm{DD}}}^2 + C_{active}(V_{DD} - V_{TN})^2 \tag{10}$$

where C_{active} and $C_{activeb}$ are the capacitance of the nodes *active* and *activeb*, respectively.

Average energy loss per cycle of power-gating circuits can be calculated as

$$E_{AV} = (E_{active})\alpha + E_{sleep}(1-\alpha) + \frac{E_{switch}}{(T_{active} + T_{sleep})/T} \tag{11}$$

where T_{active} is active time, T_{sleep} is sleep time, T is the period of the power-clock, and a is active ratio that is defined as

$$\alpha = \frac{T_{active}}{T_{active} + T_{sleep}} \tag{12}$$

The energy savings depend on active ratio, the switch sizes, and the sleep time. When *Tsleep* is long enough, the switching energy loss (E_{switch}) can be ignored, and $E_{AV} \approx E_{active}\alpha + E_{sleep}(1-\alpha)$. By increasing the gating transistor size, the average energy loss can be reduced, because E_{active} is reduced. But at small active ratio, the average energy loss can't be further reduced using large switch sizes, because E_{sleep} is increased as the switch sizes increase.

Near-threshold computing of 8-bit CAL full adders

We use an 8-bit carry-lookahead adder (CLA) based on the improved CAL circuits to show the efficiency of the gating technique. The 8-bit adder consists of six pipeline stages [4]. The six power-gating switches are inserted between the power-clock (*pc*) and virtual power-clocks (clk_1 – clk_6), respectively. This can reduce device sizes of each power-gating switch and make the layout place and route easy.

Fig. 5 shows the energy dissipation per two cycles of the improved CAL 8-bit CLA without and with the power-gating at normal source voltage. The 8-bit CLA with power-gating switches attains energy savings of 73% to 56% from 50 to 400MHz at a = 0.2

In order to obtain the maximum operation frequency and energy dissipations of the power-gating full adder in various supply voltages, HSPICE simulations have been carried out with various supply voltages and various frequencies. Maximum operating frequency of the near-threshold power-gating 8-bit adder is obtained, where the full adder has correct logic function, as shown in Fig. 6. The energy dissipations of the full adder at the maximum operation frequency are shown in Fig. 7.

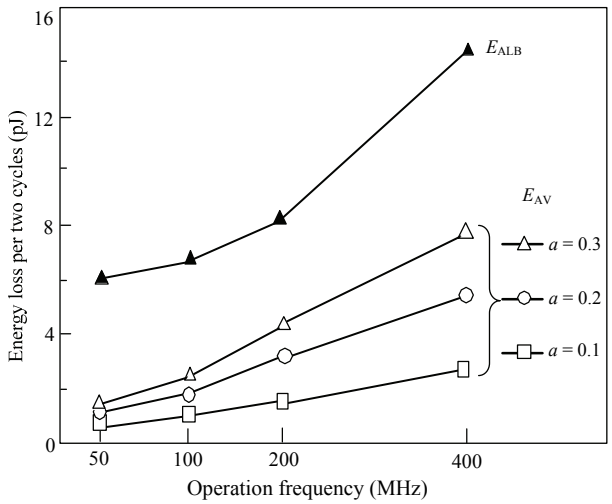

Fig.5. E_{ALB} and E_{AV} are energy consumptions of the 8-bit full adders without and with power-gating at normal voltage source, respectively. *a* is active ratio.

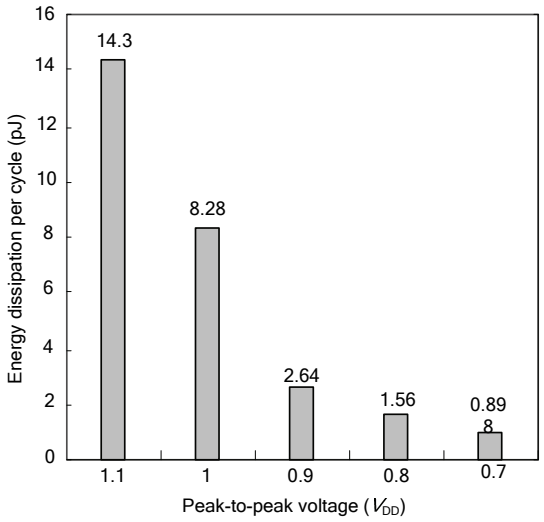

Fig.6. Energy dissipations of power-gating CAL 8-bit full adder at various supply voltage.

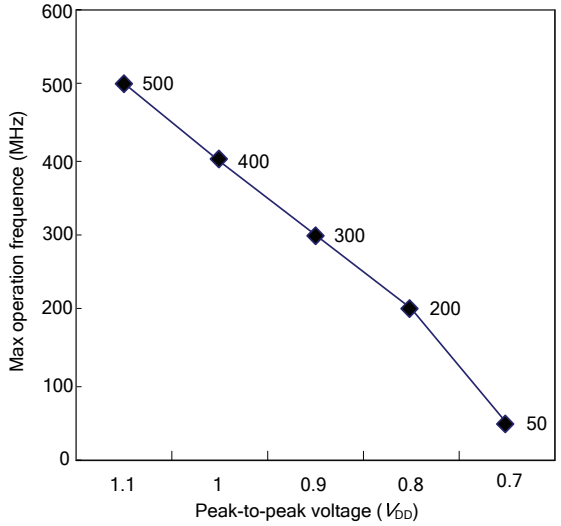

Fig.7. Max operating frequency of power-gating CAL 8-bit full adder at various supply voltage.

The maximum operating frequency is reduced as the supply voltage scales down. The proposed power-gating technique is suitable for operating on near-threshold region if ultra-low power dissipations and mid-performance application from 50MHz to 500MHz are demanded.

Conclusion

This paper introduces a power-gating scheme appropriate for near-threshold operating of single-phase adiabatic circuits. A transmission gate is used as the power-gating switch. It is inserted between the single-phase power clock and virtual power clocks to detach the power-gated logic blocks in sleep mode. A MOS bootstrapping scheme used to reduce turn-on resistors and energy overhead of MOS switches is proposed, and thus the power-gating scheme is suit for near-threshold region of adiabatic circuits. The analytical model for power-gating adiabatic circuits has also been constructed. Based on proposed model parameters, the energy overhead of the proposed power-gating scheme can be analyzed to optimize the power-gating adiabatic circuits.

CAL (Clocked Adiabatic Logic) circuits are investigated using the proposed power-gating technique with NCSU PDK 45nm technology. A near-threshold 8-bit full adder based on the CAL circuits is used to verify the proposed power-gating technique. The results show that the proposed power-gating technique is suitable for the adiabatic units operating on near-threshold region during idle periods to reduce power dissipations. The proposed power-gating technique is suitable for the adiabatic units operating on near-threshold region, which could be used for wireless sensors and biomedical applications, where ultra-low energy dissipations are demanded.

Acknowledgments

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***Authors**: prof. Jianping Hu, Faculty of Information Science and Technology, Ningbo University, E-mail: nbhjp@yahoo.com.cn; Qi Chen, Faculty of Information Science and Technology, Ningbo University, E-mail: nbuchen@yahoo.com.cn.*