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Step-up DC/DC converters for photovoltaic applications – theory and performance

Abstract. *Low voltage photovoltaic systems require highly efficient converters to deliver as much as possible energy to the load with high gain DC voltage conversion. This paper presents two efficient step-up DC/DC converters one composed of five identical phases driven interchangeably and latter partial parallel isolated converter with voltage doubler. Experimental validation of theoretical assumption and discussion on power losses has been carried out. The use of silicon carbide components, and current sharing technique assures high efficiency within wide power range.*

Streszczenie. *Systemy fotowoltaiczne wymagają stosowania przekształtników o wysokiej sprawności oraz wysokim współczynniku wzmocnienia napięcia. Publikacja prezentuje dwa podwyższające przekształtniki DC/DC: wielosekcyjny złożony z pięciu sekcji sterowanych współbieżnie oraz quasi-równoległy, izolowany z podwajaczem napięcia. Przeprowadzono eksperymentalną weryfikację teoretycznych założeń oraz dyskusję na temat strat mocy. Użycie komponentów z węglika krzemu oraz techniki dzielenia prądu wejściowego zapewniają wysoką sprawność w szerokim zakresie mocy. (**Podwyższające przekształtniki DC/DC w zastosowaniach fotowoltaicznych - rozważania teoretyczne i wyniki eksperymentalne**).*

Keywords: photovoltaic systems, step-up DC/DC converter, high voltage gain.
Słowa kluczowe: systemy fotowoltaiczne, podwyższające przekształtniki DC/DC, wysoki współczynnik wzmocnienia napięciowego.

Introduction

Among renewable energy sources, solar power has the potential to become one of the main contributor to the future electricity supply with several advantages, such as pollution-free power generation, low-maintenance cost, low-operation cost and no supply limitations [1].

Photovoltaic (PV) is direct transformation of sunlight energy into electricity. Different materials has been developed to make of a PV modules. Relatively low light to electricity power conversion ratio, reaching 30%, is the main disadvantage of commercially available PV modules. To maximisation of PV energy productivity and ensure high conversion efficiency (usually above 90% [2], [3], [4]), step-up DC/DC converter (fig.1) has to be used. Selection of the converter is critical for whole PV system power efficiency.

This paper presents the concepts of two step-up DC/DC converters dedicated for PV systems: simple multiphase step-up converter and partially parallel converter with output voltage doubler.

Low input voltage PV systems

Individual solar cells can be connected in series and/or in parallel. In order to maximize the power generation from each cell, corresponding to its particular irradiance level, the best choice is the parallel connection [3], [4], [10], [5]. This solution has the advantage over panels connection in series, because the least efficient panel does not determine the current of the whole system.

The parallel configured solar energy systems are composed of PV arrays, DC/DC step-up converter and DC/AC inverter [2] (fig.1). For that instance, total current sourcing DC/DC converter is a sum of individual panel currents.

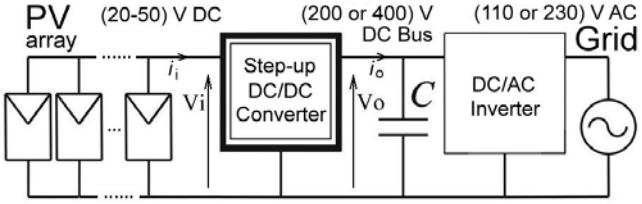


Fig.1. The array of parallel connected PV panels as the example of low input voltage system

Depending on total peak power of the PV array single converter can work with considerably high value of RMS input current i_i. In the interleaved step-up converter (fig.2) input current i_i is shared between the number of phases or balancing transformers in partial parallel converter [5]. Hence power components of single phase work with only a fraction of total input current. Conduction power losses in power transistors and diodes as well as the ones in other resistive components of the converter are directly proportional to the square of RMS current, thus they can be reduced significantly. Hence total power losses of the entire converter get reduced.

According to the electric grid standards which are in place in some countries, some grid-connected PV systems have the transformer for the galvanic isolation between the conversion stage and the grid. Without the isolation transformer, the circulation of ground current through the parasitic capacitance between the PV array and the ground may occur [6]. The DC/DC step-up converters with transformer isolation can obtain high voltage step-up trough turns ratio. Unfortunately, large turns ratio complicate transformer design. There seems to be a widespread misconception, that high transformer turns ratio is required in high gain applications. Partial paralleling of two or more isolated converters results in a reduction of the turns ratio, as well as energy losses in power switches.

Appropriate driving algorithm including Maximum Power Point Tracking (MPPT) should be implemented in converter control unit in order to assure maximisation of PV energy productivity and high conversion efficiency.

Interleaved step-up DC/DC converter

The converter comprises n identical sections connected in parallel driven interchangeably. Single section is based upon legacy flyback topology. The high efficiency of energy conversion is assured by adding up to four more sections in parallel as well as the use of SiC components. Due to non ideal coupling between L_{1k} and L_{2k} there is the leakage inductances L_{1kL} (k=1,2,...,n) and coupling coefficient K<1. Utilization of clamping diode D_{Ck} allows the input inductor leakage energy to be transferred directly to the output. D_{Ck} prevents transistor drain-to-source voltage to excess the level of V_o at transistor turn off transient. In contrary to the flyback topology [4] the windings of both primary L_{1k} and secondary L_{2k} inductors are connected together. All the transistors are driven with respect to the ground - at the low side. Required voltage gain is achieved by utilization of coupled inductors with turns ratio $N=N_{2k}/N_{1k}$ and adjusting the duty cycle of transistor gate driving signals D.

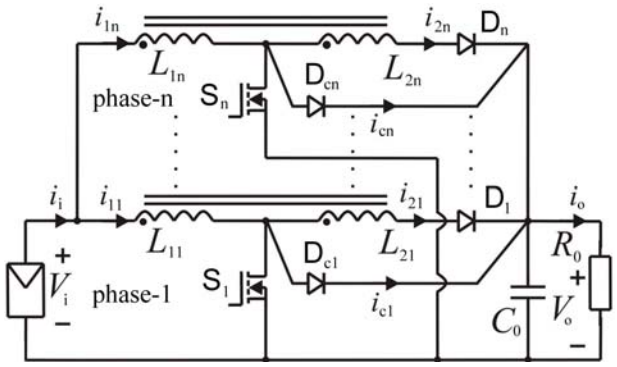


Fig.2. Step-up interleaved DC/DC converter

In continuous conduction mode there are three modes of operation in one switching cycle *T* of interleaved step-up DC/DC converter (fig.3). Assuming that all the phases are composed of identical components, at the example of k-th phase (k=1,2,...,n) in mode-1, when transistor S_k is switched ON, the energy is transferred from input to the primary inductance L_{1k} and leakage inductance L_{1kL}. According to figure 3d in this mode the slope of L_{1k} current can be described as:

$$(1)\quad \frac{\mathrm{d}\, i_{1k}}{\mathrm{d}\, t} = \frac{V_i}{L_{1k} + L_{1kL}}, \qquad t = (t_0 - t_1)$$

Since:

$$(2)\quad L_{2k} = N^2 \cdot L_{1k}$$

$$(3)\quad M = K \cdot \sqrt{L_{1k} \cdot L_{2k}}$$

$$(4)\quad L_{1kL} = L_1 - \frac{M}{N}$$

where M is L_{1k} and L_{2k} mutual inductance. The leakage inductance can be derived from (2) to (4) and defined as:

$$(5)\quad L_{1kL} = L_1 \cdot (1 - K)$$

and a modified equation (1) can be presented as:

$$(6)\quad \frac{\mathrm{d}\, i_{1k}}{\mathrm{d}\, t} = \frac{V_i}{(2 - K) \cdot L_{1k}}, \qquad t = (t_0 - t_1)$$

The energy stored in leakage inductance is discharged to output capacitor C_0 through forward biased diode D_{Ck} in mode-2.

$$(7)\quad \frac{\mathrm{d}\, i_{1kL}}{\mathrm{d}\, t} = \frac{V_i - V_0}{L_{1kL}} \cdot \frac{N}{N+1}, \qquad t = (t_1 - t_2)$$

In mode-3 when the leakage inductance current value is zero, transistor S_k is turned off and the output diode D_k is on, the slope of primary inductance current is:

$$(8)\quad \frac{\mathrm{d}\, i_{1k}}{\mathrm{d}\, t} = \frac{V_i - V_0}{L_{1k}} \cdot \frac{1}{N+1}, \qquad t = (t_2 - t_3)$$

Neglecting the leakage energy during $t=(t_1,t_2)$ and using the principles of coupled inductor volt-second balance [7] the voltage gain of the converter can be defined as:

$$(9)\quad \frac{V_0}{V_i} = 1 + \frac{D(1+N)}{(2-K)\cdot(1-D)}, \qquad 0 < D < 1$$

Figure 3 describes the work of n=3-phase converter. The gate driving signals of transistors S_1, S_2 and S_3 are phase shifted by $2\pi/3$ electrical angle and switched at duty cycle D=66% (fig.3a, 3b and 3c).

Aggregate output current (i_o) is composed of each individual phase currents (fig.3h) and is further filtered by C_0. According to (9) output voltage (V_o) regulation can be achieved by adjusting the duty cycle of the switches.

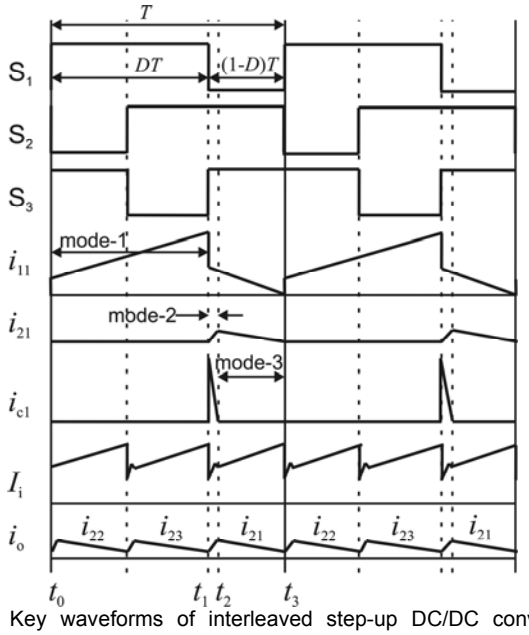


Fig.3. Key waveforms of interleaved step-up DC/DC converter during operation modes 1 to 3

Interleaved phase driving leads to reduce input current ripples. By integrating (6) in steady-state single phase input current ripple is defined by equation 10:

$$(10)\quad \Delta i_{1k} = i_{1k\_max} - i_{1k\_min} = \frac{V_i \cdot D}{(2-K)\cdot L_{1k} \cdot f_S}$$

where f_S is single phase switching frequency and 0<D<1.

As n working phases are shifted in time domain by $2\pi/n$ electric angle overall input current ripples get cancelled. Thus magnitude of multi-phase converter input current ripples is reduced comparing to single phase one. Figure 4 depicts reduction of overall input current ripple of multi-phase converter in relation to single-phase one versus variation of duty cycle of each phase current.

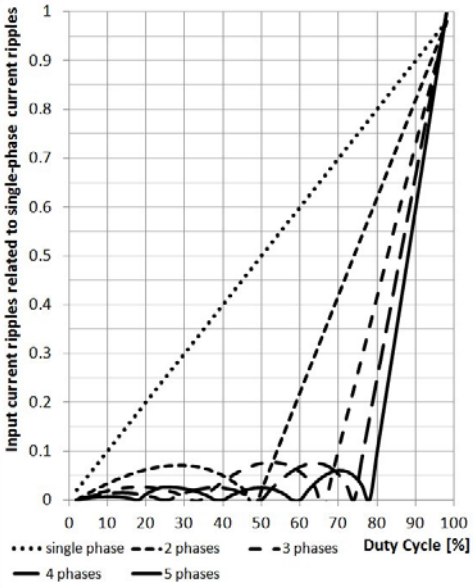
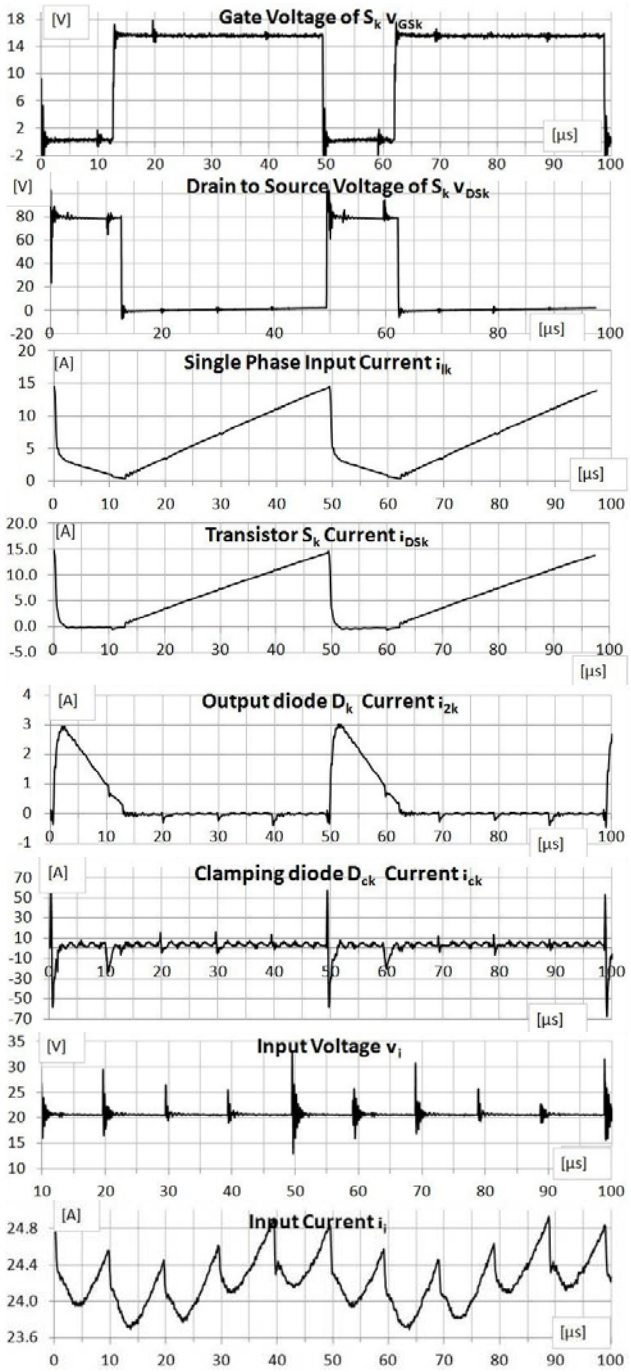


Fig.4. Input current ripples of multiphase interleaved converter related to single-phase input current ripples vs. duty cycle

In terms of input current ripple reduction it is essential to keep duty cycle below 70%, while working with 3 to 5 phases. For the same reason interleaved driving scheme allows to reduce output voltage ripples. Effective switching frequency is n times higher than single-phase switching frequency f_S. Higher reliability and power density of the system can be obtained furthermore.

Interleaved step-up DC/DC converter experimental verification

The prototype of 5-phase interleaved step-up converter has been developed and tested. The coupled inductors are designed with Super-MSS core. Their primary winding inductance L_{1k}=64 μH, turns ratio of N=3 and inductance coupling coefficient K=0.97. Input leakage inductance L_{1kL} is 1.9 μH. Table 1 lists other converter's components. For all tests the switching frequency f_S is 20 kHz. Figure 5 presents measured waveforms of tested converter.



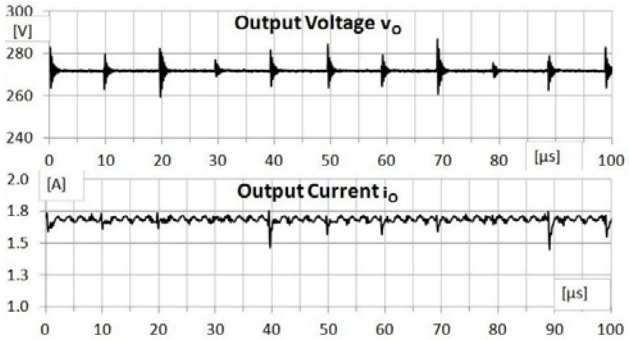


Fig.5. 5-phase interleaved step-up converter experimental waveforms at 500W of output power and 75% of duty cycle

During turn off transient, transistors are exposed on high voltage spikes not exceeding V_o rail, so high drain-to-source voltage transistors need to be used.

Table 1. Interleaved converter components

Component	Symb.	Type	Specification
Power transistor	S_k	CMF20120D	80 mΩ /1200 V
Output diode	D_k	C2D20120	20 A /1200 V
Clamping diode	D_{ck}	HFA25TB60	10 A /600 V
Output capacitor	C_0	HE2G477M35040	2x470 uF/400 V

Driving circuitry consists of optocoupler followed by MOSFET transistor driver TC4221 and the gate driving network comprising C_g (10 nF), D_g (BAS16), and R_g (10 Ω) all in parallel decided to optimize turn off time of the transistors.

Figure 7 to figure 11 depict results of efficiency and voltage gain measurements of tested converter at 600 W of output power.

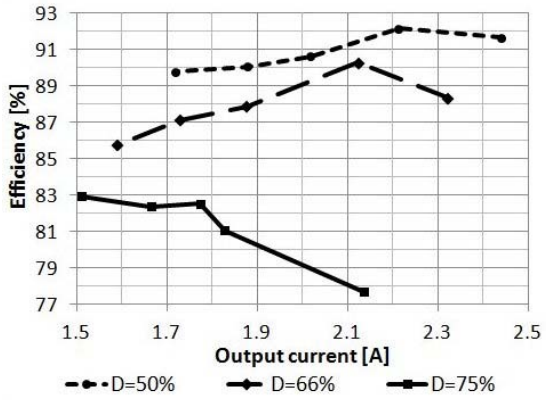


Fig.7. Efficiency vs. output current and different duty cycle of 3-phase interleaved step-up converter

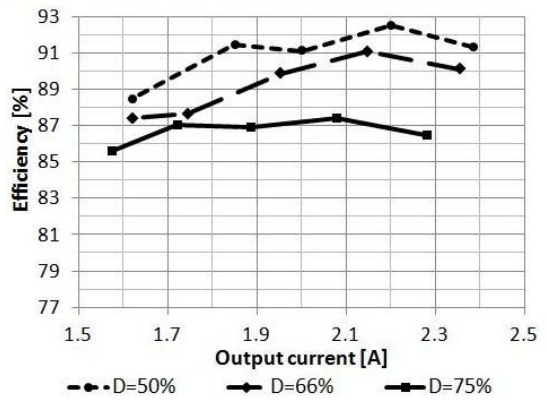


Fig.8. Efficiency vs. output current and different duty cycle of 4-phase interleaved step-up converter

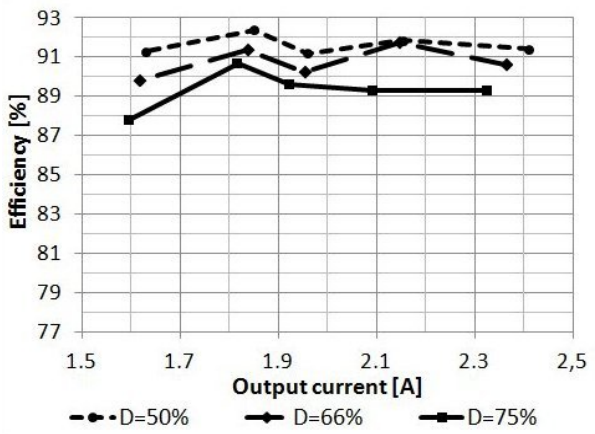


Fig.9. Efficiency vs. output current and different duty cycle of 5-phase interleaved step-up converter

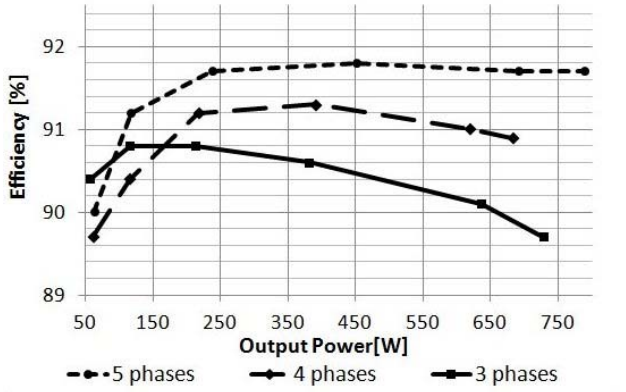


Fig.10. Efficiency vs. output power at duty cycle of 66%, at fixed load resistance of 117 Ω

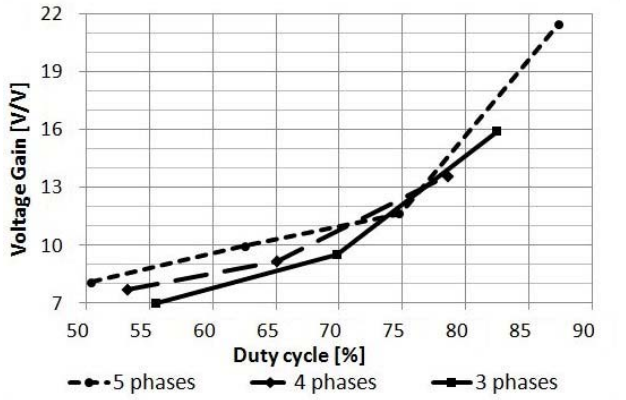


Fig.11. Voltage gain vs. duty cycle at fixed load resistance of 117 Ω

However maximum efficiency can be achieved at lower values of duty cycle (i.e. 50%) (fig.7 to fig.9) DC voltage gain only up to 8 can be reached (fig.11). To increase voltage gain higher duty cycle needs to be applied which effectively decreases the efficiency according to figure 7 to figure 9. Nevertheless the voltage gain above 9 can be reached for 3, 4 and 5 phases working with duty cycle not exceeding 66% (fig.11) where with 5 phases working the converter demonstrates high efficiency above 91.5% within wide power range (fig.10). For lighter loads below 100 W roughly 3-phase or 4-phase configuration may be used to maintain highest efficiency possible (fig.10).

Partial parallel isolated DC/DC step-up converter

Partial parallel isolated DC/DC step-up converter with voltage doubler topology is depicted in figure 12.

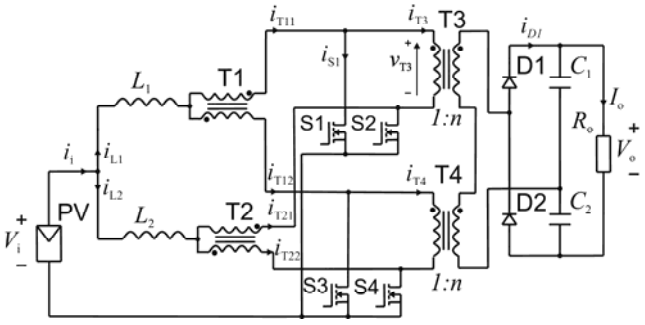


Fig.12. Partial parallel isolated DC/DC step-up converter with voltage doubler

High input current i_i is divided equally into two smaller currents i_{L1}, i_{L2}. Balancing transformers T1, T2 further split currents flowing through the input inductors L_1, L_2. As a result both transistors pairs (S1, S4 or S2, S3) of the converter conduct only half the input current. When the current i_{L1} is rising the current i_{L2} is falling, except the overlap time (S1, S2, S3, S4 in conduction state) when they are both rising. Both parallel connected half-bridges form first section of voltage step-up. Transformers T3 and T4 assure galvanic isolation between two power stages. The output diode rectifier (D1, D2) with capacitors (C1, C2) double rectified AC voltage of serial connected secondary T3 and T4 transformer windings.

Each balancing transformer (fig.13) splits input inductor currents i_{L1}, i_{L2} into two smaller currents (i.e. i_{T11} and i_{T12}). These smaller loops only need to switch half of the input current, thereby achieving much faster current switching. Current balancing transformers in combination with serial connection of secondary windings of isolation transformers guarantee current sharing between all converter transistors. Two parallel power stages operate as parts of two individual half-bridge converters which share input current and power level.

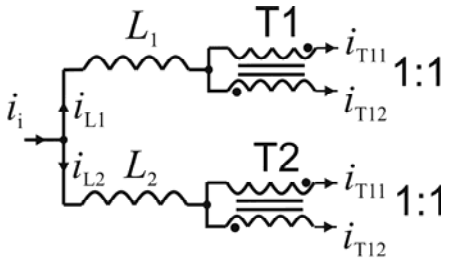


Fig.13. Input storage inductors and arrangement of current balancing transformers

The input current in one stage exactly matches the current in the parallel branch, therefore there is no need for additional control to guarantee current balancing between power stages.

In this topology, primary power stages share the same control signals with same phase switching sequence for the corresponding switches which allows a simpler control. Output diodes as well as output filters are common to both of the primary stages.

There are three basic modes of operation of the converter. In these time intervals, the energy is stored in input inductors, or transmitted to the load. Theoretical waveforms of the isolated DC/DC step-up converter with voltage doubler are illustrated in figure 14.

(t_1) - transistors S1, S4 are turned off; transistors S2 and S3 are in the conduction state, transformer T3 primary side voltage v_{T3} reaches maximum value, diode D1 begins to conduct, input current i_i reaches maximum value

(t_1-t_2) - transistors S1, S4 are turned off; S2 and S3 are conducting, the currents i_i , i_{L1} are falling i_{L2} is rising
(t_2) - transistors S2 and S3 are in the conducting state transistors S1, S4 begin to conduct, input current i_i reaches minimum value each transistor current is equal to a quarter of the input current
(t_2-t_3) - all transistors are in conduction state, primary side of transformer T3 voltage drops to zero, input current i_i rises
(t_3) - similar to (t_1), transistors S2, S3 are turned off; transistors S1 and S4 are in the conduction state
(t_3-t_4) - similar to (t_1-t_2) except that currents i_i, i_{L2} are falling and i_{L1} is rising

Duration of each operation mode depends on the duty cycle *D*. V_i in series with L_1 and L_2 act as DC current source which supply power converter therefore value of the duty cycle has to be greater than 50%. This will ensure the proper work of the converter.

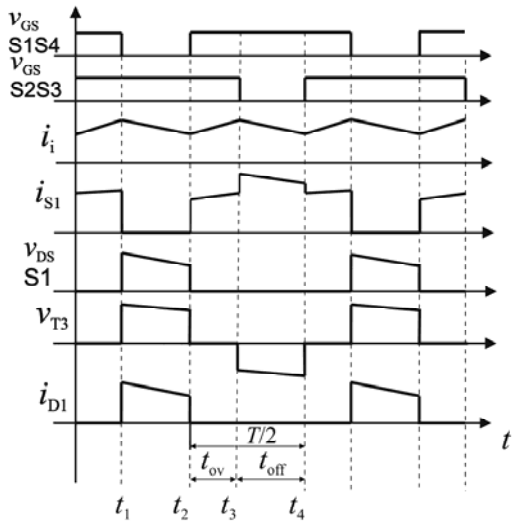


Fig.14. Typical waveforms of partial parallel isolated DC/DC step-up converter with voltage doubler

All transistors are driven at the same time (t_{ov}) or in pairs S1, S4 and S2, S3 (t_{off}). The sum of all transistor drive time and drive time of transistor pair is equal to half of the period.

(11) $$T = 2(t_{ov} + t_{off})$$

The *d*, determines the overlap ratio.

(12) $$d = \frac{2t_{ov}}{T}$$

Voltage transfer function of the converter is equal

(13) $$B = \frac{V_o}{V_i} = \frac{4n}{1-D}$$

where duty cycle is

(14) $$D = d + \frac{t_{off}}{T} = \frac{(2t_{ov} + t_{off})}{T}$$

In low-voltage high-power converters conduction losses in transistors dominate due to high input currents. They increase with duty cycle [9] and proportionally with transistor $R_{DS(on)}$.

Due to the high input current, transistor conduction losses are dominant in high-power low-voltage converters. Thus optimal design and selection of transistors are obviously very important in achieving high conversion efficiency. Power MOSFET on-resistance ($R_{DS(on)}$) increases exponentially with rated drain-source breakdown voltage (15) [13].

(15) $$R_{DS(on)} \propto V_{(BR)DSS}^{2.5to2.7}$$

Any possibility of reducing transistors voltage stress and consequently $V_{(BR)DSS}$ voltage will reduce conduction losses and thus significantly increase converter efficiency. It is very important that the voltage on both half-bridges transistors is to be kept as low as possible.

Partial parallel isolated DC/DC step-up converter experimental verification

The prototype of partially parallel isolated DC/DC step-up converter with voltage doubler was developed to confirm theoretical assumptions. Solar panels with desired output voltage and current were simulated by adjusted voltage source. Table 2 lists the components used in the construction of the converter.

Table 2. Partial parallel converter components

Component	Symb.	Type	Specification
Power transistor	S1-S4	IRFP4468	2 mΩ /100 V
Output diode	D1-D2	SDT12S60	12 A /600 V
Input inductor	L_1-L_2	DTP	22 uH /120 A
Balancing transform.	T1-T2	TI-T63-4-4	Turns ratio 1
Isolation transform.	T3-T4	TI-T87-6-12	Turns ratio 2
Output capacitor	C_1-C_2	B32926	2x10 uF/305 V

Transistor control signals of constant 40 kHz frequency were generated in Cyclone III FPGA. The same as in case of interleaved converter transistor driving network has been utilized.

Since the rectifier diodes are placed directly across the output capacitors, diode reverse voltage must be equal or greater than the desired output voltage. SiC Schottky diodes were used in output rectifier, since they do not suffer from reverse recovery and turn off much faster than conventional Si diode of similar voltage/current ratings.

By using low $R_{DS(on)}$ MOSFET transistors, the converter conduction power losses were relatively small even at large input currents. They grow with the duty cycle increase as it can be seen in diagrams below. However satisfactory value of the voltage gain (12 and more) can be achieved for D from the range of 55% to 60% at the input voltage of 30 V. Input inductors maintain input current ripple at the desired level and store energy during overlap.
Figure 15 shows measured values of voltages and currents at 30 V of input voltage and 140 Ω of output load with a duty cycle of 60%.

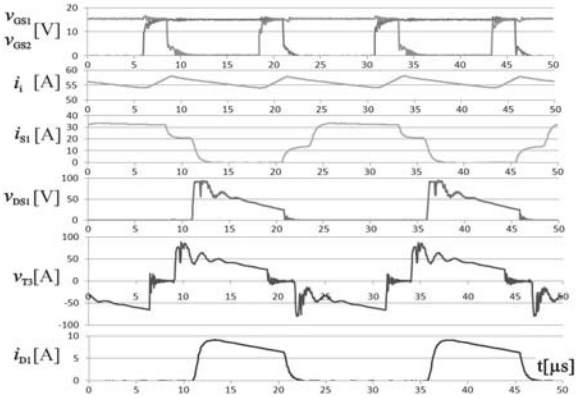


Fig.15. Measured converter waveforms at 30 V input voltage and duty cycle D=60%

Measured waveforms reflect theoretical assumptions. Overshoot of v_{DS1} voltage has been observed for all the transistors of the converter. It is related to the leakage inductances of the isolation transformers. Turn-off voltage

overshoot of the transistors will increase their switching losses. The same overvoltage is visible in transformer T3 primary side voltage v_{T3}.

Diode current i_{D1} and transistor current are not decayed by parasitic overshoots. The driving signal (v_{GS1}, v_{GS3}) voltage overshoots are present due to charging of parasitic capacitances. Observed 7% ripple of the input current i_i is satisfactory result.

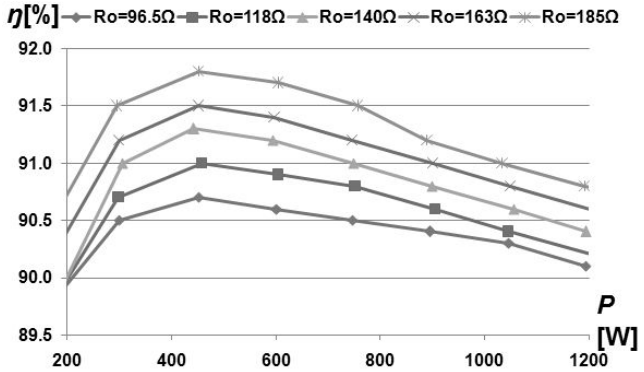


Fig.16. Efficiency η versus output power P_o or different load resistances and fixed duty cycle of D=55%

In figure 16 and figure 17 efficiency and voltage gain plots are shown for different values of the output current. The highest converter efficiency 91.8% (fig.16) was achieved at 28.5 A of input current and 451.8 W output power and output resistance of 185 Ω.

For all output resistances efficiency exceeded 90% in output power range (200-1200) W.

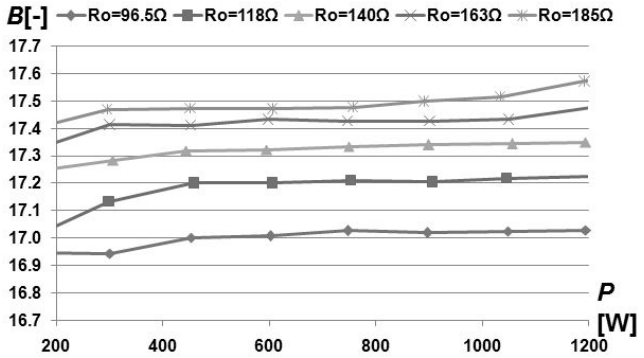


Fig.17. Voltage gain B versus output power P_o for different load resistances and fixed duty cycle of D=55%

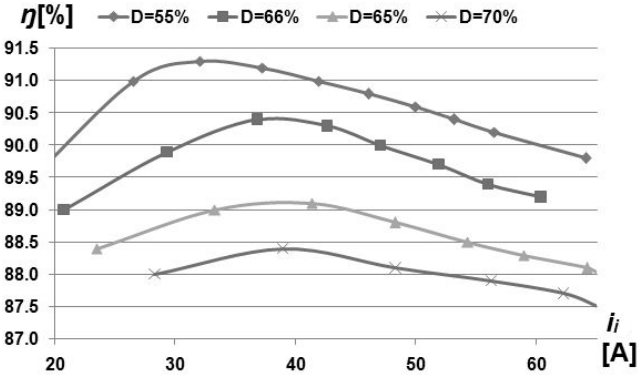


Fig.18. Efficiency η versus input current i_i for different duty cycles D and fixed output resistance of 140 Ω

Voltage gain varied from 16.9 to 17.6 along with load conditions. One can therefore conclude that the system maintains an approximately constant high voltage gain despite load changes. With such a large voltage gain ratio, 24 V solar modules connected in parallel will provide required voltage level to proper inverter operation with the assumption, that they will be held in their maximum power point.

Figure 18 shows efficiency plots for different values of duty cycle as a function of input current. It can be seen that the highest efficiency 91.3% was achieved for duty cycle of 55% and input current 32.1 A. Within the input power range of (200-1200) W voltage gain above 17 was reported.

With the increase of duty cycle, the input current also increases and therefore the efficiency of the hard switched converter decreases. In the case of operation with real photovoltaic panel MPPT control algorithm is crucial to ensure maximum utilization of the supplied power with the maximum current at the lowest possible values of duty cycle.

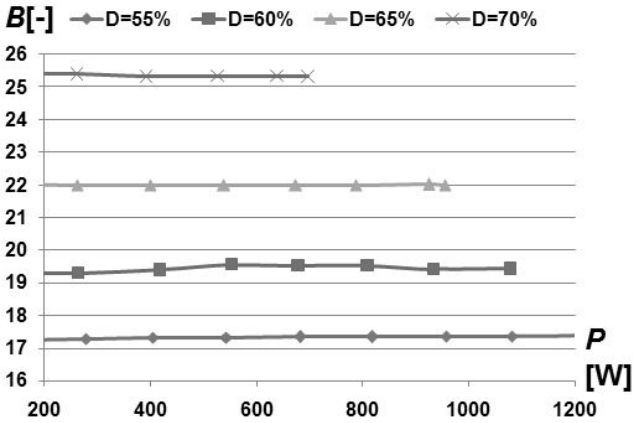


Fig.19. Voltage gain B versus output power P_o for different duty cycles D and fixed output resistance of 140 Ω

The highest voltage gain of 25.4 (fig.19) for converter working with 70% duty cycle and efficiency over 88% assures desirable level of output voltages even at very low input voltage. The price for such a significant voltage gain is the lower energy conversion efficiency, however, at very low input voltage it may be considerable.

Efficiency analysis of step-up DC/DC converters

Due to improve the efficiency of power converter it is essential to analyze the sources of power losses. The major part of transistor device power loss shares conduction loss which is proportional to square of RMS value of current and transistor's $R_{DS(on)}$ resistance. Switching losses are other source of semiconductor power losses occurring while device current overlaps voltage during turn on and turn off transients. The losses in connecting wires and ones in magnetic component windings, core losses as well as input and output capacitor ESR losses have also their share in total power loss budget of the converter. The control and driving losses also need to be considered [10]. Table 3 collates experimentally measured or estimated cumulated loss distributions of both converters at 500 W of output power. 5-phase interleaved converter worked at 75% of duty cycle. For that conditions totally 46 W of power was dissipated within entire converter. Partial parallel isolated converter's total power losses were at the level of 40 W and duty cycle of driving signal was 55%.

Table 3. Cumulated power loss distribution of both converters: a) interleaved converter and b) partial parallel isolated converter

	Parameter	a)	b)
1	MOSFET total power losses	51.5 %	40.4 %
2	Total diode power losses	9.9 %	9.8 %
3	Total inductor core losses	8.0 %	14.4 %
4	Total inductor copper losses	20.9 %	24.4 %
5	Other losses (including capacitor ESR, gate drive, PCB tracks)	9.7 %	11.0 %

In the interleaved converter despite SiC switches with lowest $R_{DS(on)}$ used around half of total power is dissipated within transistors. To use the transistors with even lower $R_{DS(on)}$ and lower voltage ratings, common active clamp circuitry needs to be developed [8], [9] which in turn complicates the design. In the partial parallel converter total transistor power losses share significant part (40.4%) in its power loss budget. To minimize transistor switching losses soft switching technique [12] needs to be developed.

In case of partial parallel converter around a quarter (24.4%) of total power is dissipated in magnetic component's copper. Around 20% power is dissipated in coupled inductors copper in the interleaved converter. To improve converter's efficiency it is essential to improve transformer design or apply planar transformers instead [11].

Careful PCB design and proper capacitor choice lead to reduce power losses in resistive design components.

For both converters the measurements of power, efficiency, and voltage gain were performed using Hioki 8855 Data Recorder.

Conclusion

The prototypes of two proposed converters have been developed and analysis of power losses and the discussion on how to minimize the power losses of the converters has been carried out. The experimental results of developed prototypes have been presented for validation. Despite hard switching technique both developed prototypes demonstrated over 91% of power efficiency within wide output power range. Current sharing technique and use of coupled inductors and balancing transformers demonstrated possibility of power losses reduction and thus efficiency improvement. High voltage gain over 10 was reported which enables both topologies to be applied in low voltage PV systems.

Partial parallel converter demonstrated conversion efficiency over 90% within wide power range, peak efficiency reaches 91.8 %. Voltage gain varied from 17 to 25 at very high input currents what allows converter to work with low voltage solar panels. For interleaved converter the peak efficiency reached 92.6% with 5 phases working at duty cycle of 50% despite hard switched transistor operation. The number of working phases can vary depending on the load requirements to secure highest efficiency especially at light loads.

Easily adaptable driving scheme and simple topology along with high enough efficiency make proposed converters a good choice to apply in low voltage photovoltaic systems.

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