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An Integrated Analog Demultiplexer for Spatial Multiplexing of Local Elements Scheme Using MOS Transistors

Abstract. *This paper proposes a CMOS analog demultiplexer for Spatial Multiplexing of Local Elements scheme at baseband level. This technique is a front-end receiver architecture which uses only one RF channel, carrying multiplexed information from multiple antennas into one RF single channel. The described circuit has four channels, in which each channel has a differential switch pair and an OTA for amplification and differential to single-ended signal conversion. The specifications and simulation performance are in close agreement, which validate the proposed compact design.*

Streszczenie. *W artykule zaprezentowano analogowy demultiplekser CMOS do przestrzennego multipleksowania (Spatial multiplexing). Ta technika jest stosowana w odbiornikach używających tylko jeden kanał RF i umożliwia multipleksowanie informacji z wielu anten. Opisany układ ma cztery kanały i każdy z kanałów ma różną parę kluczy.**(Scalony multiplekser analogowy CMOS dla techniki Spatial Multiplexing)***

Keywords: Demultiplexer, CMOS, Integrated Circuit, SMILE scheme.
Słowa kluczowe: demultiplekser, CMOS, sieci bezprzewodowe.

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Introduction

The steady growth of the CMOS technology to implement integrated circuit has been shown as a trend in the design of new devices to cater the increasing demand for mobile communications systems, which currently comprise a wide range of services, including: Mobile system, personal mobile service, satellite, and specialized mobile radios (used by the police, firemen, army, etc.). Therefore, the CMOS technology has been gradually placed in the manufacturing of devices for systems operating standards like WCDMA, GSM, WiMAX, Wi-Fi, Bluetooth, ZigBee, among others, and becoming the working target for designers [1].

Receiving antenna arrays on these standards [2] typically have signal processing performed on baseband. This requires that the amplitude and phase of the signals become properly converted from the antennas to the subsequential stages and vice-versa. In this way, for conventional receivers, an independent set of active RF circuits (LNA and mixer) is required for each channel. Thus, the hardware becomes more expensive contrasting with the growth of low cost wireless systems, considering that the price and power consumption are proportional to the number of the elements in the array.

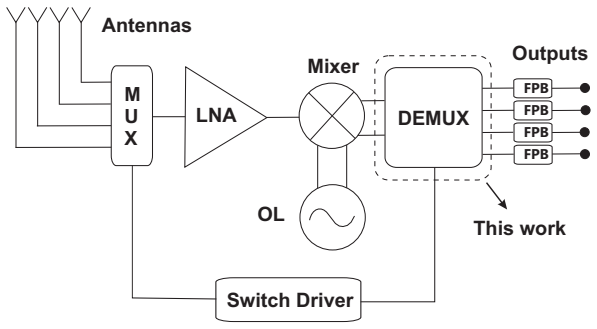


Fig. 1. The SMILE technique diagram.

Another issue is that the arrays with multiple power lines and nontrivial RF circuits are responsible for introducing noise into the system, besides impairing the integration in small areas. Many efforts have been expended in order to reduce the repetitive use of RF channels. The works [3, 4] show some of these attempts, but in limited environment and system conditions. On the other hand, a quite attractive configuration employs the SMILE (Spatial MultIplexing of Local Elements) technique [5, 6] which is shown in Fig. 1.

The aim of this technique is to reduce the number of required RF channels for just one, without loss of signal fidelity. This is achieved by switching individually the elements of the array (antennas) at a frequency above the bandwidth. This is equivalent to sample a modulated carrier using sequential pulses [7].

The spatially sampled signals are then multiplexed to form a single output, similar to the TDMA. Once amplified and converted to the baseband, the channel is demultiplexed and the signals recomposed, applying to them a low-pass filter array, without loss of fidelity based on Nyquist sampling law. Then, the signals are digitized to apply the digital signal processing as typically occurs in smart antenna system. A DBF (Digital Beam Forming) algorithm can be applied for example, for the beam selection at the signal reception, in such a way to minimize the interference and improve the quality and sensitivity of the received signal by the system.

The frequency spectrum due to the switching imposed by the SMILE technique for each channel of the system is shown in Fig. 2, where it can be seen that the envelope of points follows a $|Sa(x)|$.

The component frequencies are fixed spacing due to the periodic sampling of the signal with constant frequency $f_s = 1/T_s$. For an array with N elements, the following condition, $f_s = 1/T_s = 1/N\tau_s$, must be observed. To avoid signal aliasing, the sampling rate is set to one-sided bandwidth *B*, as:

$$f_s \geq B \times N \tag{1}$$

Once multiplexed, the channels from the respective antennas become a single RF channel, which is amplified and converted to the baseband. Then, an analog demultiplexer (which is switched by the same signal of the RF multiplexer, thereby avoiding the occurrence of jitter in the signal) is used to separate the different channels of the system.

In order to obtain the original signal, the cutoff frequency of the low-pass filter is determined in such a way, that only the fundamental frequency of the channel does not have attenuation, i.e.:

$$B < f_{fpb} < f_s - B \tag{2}$$

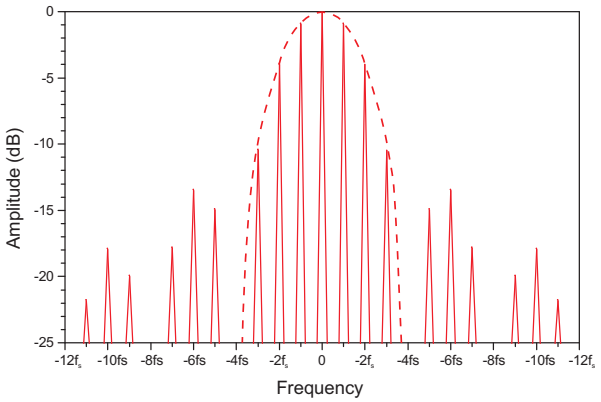


Fig. 2. Baseband frequency spectrum of a SMILE scheme.

In this context, the aim of this work is the design of a baseband analog demultiplexer for SMILE scheme, as shown in Fig. 1. The CMOS technology used for its complete implementation is $0.35\mu m$ from Austriamicrosystem foundry .

This paper is organized as follows: Besides this introduction, in Section II, the proposed CMOS analog demultiplexer is shown and designed. In Section III, the simulation results are analyzed, showing its good performance. In addition, in Section IV, it is described the layout. Finally, the Section IV concludes this work.

Analog Demultiplexer

In a SMILE scheme, after the frequency translation, there is a baseband signal containing information from all channels. Thus, this one needs to be demultiplexed, so that each channel can be separately analyzed by a management system. As usually the output of the mixers is balanced, the demultiplexer needs to be compatible, and also perform the conversion of a signal from a balanced configuration to an unbalanced one. Therefore, it is selected for this proposed implementation a system of NMOS switches to perform the demultiplexing of the balanced signal, and a OTA (Operational Transconductance Amplifier) [8, 9] with configuration of differential amplifier as the last stage of voltage gain and signal conversion for each channel.

As the OTA has a limited frequency range [10], it attenuates the higher frequency components of the spectrum if the switches are located after it. In this way, it is necessary to perform the demultiplexing of the channels through the differential analog switches before the OTAs. The differential signal, already demultiplexed, can be applied in the OTAs, which have the role of an active balanced-unbalanced converter for demultiplexed baseband signals. Thereby, each channel of the demultiplexer is constructed by a set of analog switches and differential OTA as shown in Fig. 3.

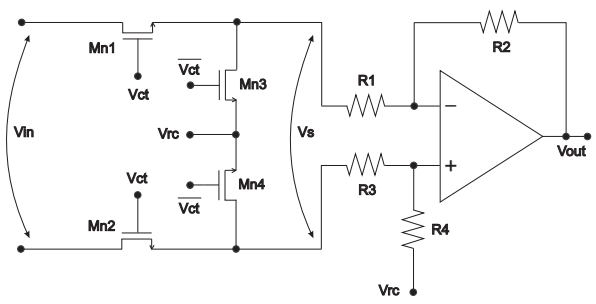


Fig. 3. Schematic of the analog demultiplexer - one channel only.

For the proposed system with four channels, a demultiplexing system composed by four independent channels is designed, i.e. a quadruple replication of the system proposed in Fig. 3. The analog switches that use NMOS transistors are often employed for signal commutation in several applications [11]. It can be observed in this circuit that the switch is composed by a main switching function NMOS transistor, coupled to a shunt transistor to increase the switch isolation at the *OFF* state [12, 13]. The switch is driven by a 3.3 V, and also by a complementary signal, in order to trigger the shunt transistor in a complementary way.

The transistors of the differential NMOS switch (Mn1 and Mn2) were picked in order to ensure high reverse insulation, maintaining good linearity and insertion loss as low as possible in the operating range [14, 15]. These NMOS transistors must operate in the cutoff region ($V_{gs} \leq V_{th}$), with high resistance at *OFF* state, and must operate in the linear region ($V_{ds} \leq V_{gs} - V_{th}$ and $V_{gs} \geq V_{th}$) to represent a low series resistance at *ON* state.

The equation 3 presents the resistance of a NMOS transistor in the linear region:

$$r_{ds} = \frac{1}{KPN\left(\frac{W}{L}\right)|V_{gs} - V_{th}|} \tag{3}$$

The length of the switching transistors must be the smallest permitted by the technology, in this case 0.35μm, in such way to maximize switching speed. On the contrary, the width must be the greater as possible, but from a certain value of W the parasitic capacitances begin to degrade the circuit operation. The increase of the capacitive coupling with the substrate results in higher transmission losses. Thus, the optimized value found through simulations for the relationship W/L is 170/0.35, whereas multiple fingers were employs in order to minimize gate resistances and parasitic effects in source and drain [16]. The shunt transistors dimensions are not a critical issue [17, 18], thereby the relationship 40/0.35 is chosen, which ensures the good insulation found in this design.

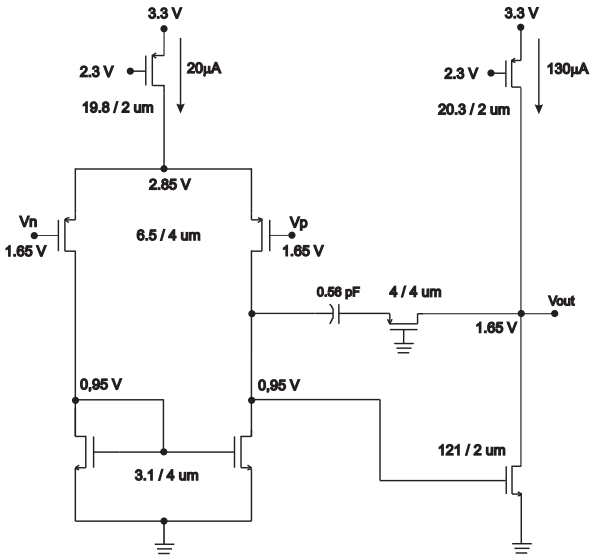
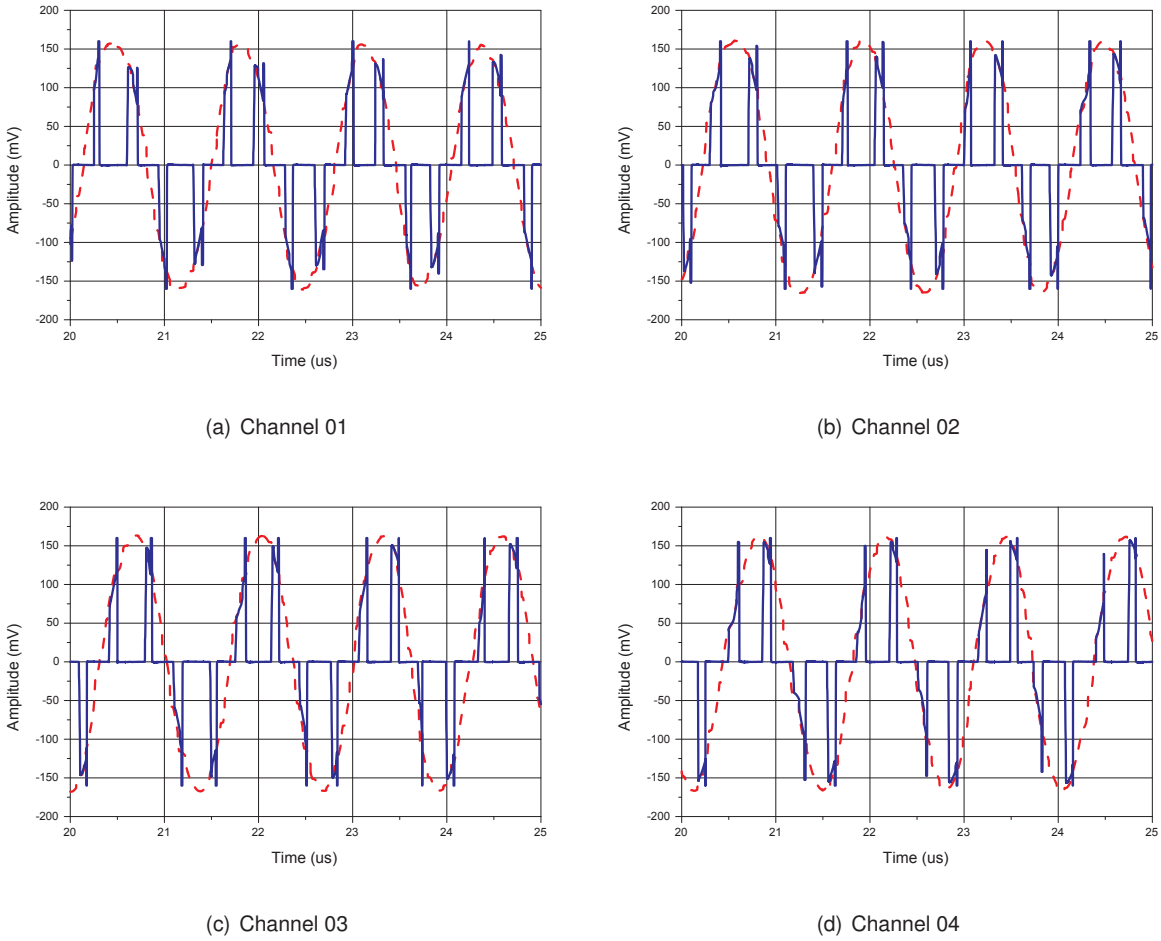


Fig. 4. Schematic of the OTA.

The complete schematic of the OTA, including the Miller compensation is shown in Fig. 4, where is also provided an overview of the transistors polarization and (W/L) sizes. The scheme consists of a differential input stage with active load and a second stage with a common source type and current sources. The circuitry towards generating the bias voltages



(a) Channel 01

(b) Channel 02

(c) Channel 03

(d) Channel 04

Fig. 5. Output signals for the analog demultiplexing system for a 30° array angle.

have been omitted in order to clarify the visualization of the schematic.

Differentially from conventional OTAs, in which a symmetrical power supply is used, so that, the input and output are referenced to the ground, this OTA uses a single supply voltage referenced to ground. Thus, the circuit must operate with a DC offset of 1.65V [19].

Demultiplexer results and analysis

During the optimization stage, the corner analysis responses are obtained with a standard load of 10kΩ and 10pF connected to output. They are summarized in Table 1. From the obtained results, it can be observed that the values after optimization show a good operability of the amplifier with stability (Phase margin analysis) and adequate DC gain.

Table 1. OTA frequency response with corner analysis.

OTA Parameters	f_1 (kHz)	*GBW* (MHz)	*PM* (○)	*DC gain* (dB)
Typical	10	8.41	65.15	59.42
Slow	7.5	5.96	71.95	58.40
Fast	15	11.89	60.93	59.82

The OTA is configured as a differences amplifier, as shown in Fig. 3. In this way, after deducting the gain expression, it can obtain G=-R2/R1 V/V for simplified case, where the relationship R3=R1 and R4=R2 is adopted. This circuit uses 50kΩ and 10kΩ, which represent a voltage gain of 5V/V at this stage.

The results of four output SMILE channels with a 30° excitation angle are shown in Fig. 5. The input multiplexed signal used as reference can be observed in Fig. 6. This angle is chosen due to ones beyond 35° normally present an additional signal attenuation in real experiential tests. This characteristic is due to antenna elements' directive radiation pattern.

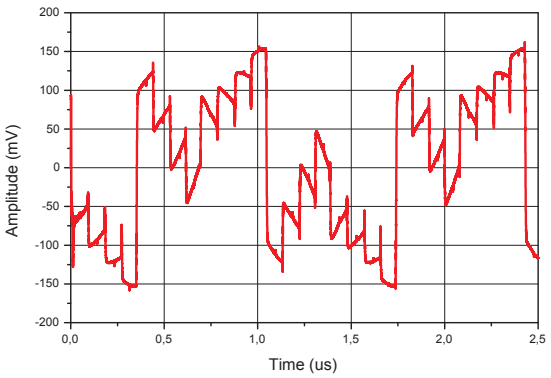


Fig. 6. Input signal of the demultiplexer for 30° antenna array angle at the SMILE scheme.

At this one, all array elements are reached by a electromagnetic wave 30° out of phase. It increases the band of the multiplexed signal maximizing the performance of this test. The envelope lines represent the output of a low-pass filter array used for recovered the demultiplexed signals to

original ones. A phase progression of 30° through the four channels can be observed, showing the demultiplexer ability to correctly retain array element phasing through demultiplexing process.

Layout

To avoid offset problems in the design of the amplifier components, the match between then must be carefully done. The random offset is provided by mismatches between the match pair of the amplifier input stage, respectively, the input differential pair and the pair of active load. These mismatches are related to variations in the thickness of the gate oxide, gradients of impurities in the transistors, and distortions related to thermal gradients [20]. Although these factors not being manipulated by the designer, there are some layout strategies to minimize them.

Thus, there are basically two rules to be followed: first of all, transistors must be placed as close as possible to decrease the gradient, and then apply the common centroid configuration, which ensure that the gradient affect all transistors in the same manner [21]. In this work, the cross-quad technique [22] is used, where the transistors pair is split in four new transistors.

The layout of one demultiplexer channel (note that the full demultiplexer system is composed by four interconnected parallels channels in an independently way, sharing only the same input signal) is shown in Fig. 7. It can be observed the set of two switches on the left side, and a OTA using a differential pair implemented with cross-quad topology technique on the right side. Also, it is clear the presence of the resistors used for the differences amplifier configuration. These resistors (10kΩ and 50kΩ) are implemented using RPOLYH.

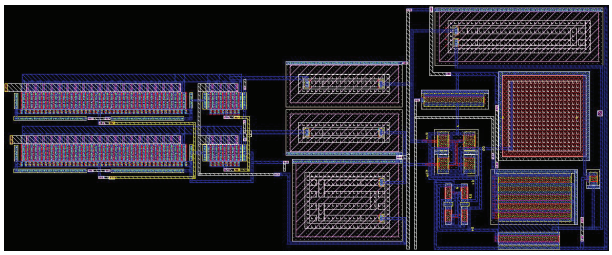


Fig. 7. Analog demultiplexer layout (one channel only).

Conclusion

In this paper is presented an analog demultiplexer integrated in CMOS technology employed in the Spatial Multiplexing of Local Elements Technique. This circuit is composed by a set of differential MOS analog switches, followed by an OTA, for the signal conversion and amplification. The obtained results were extremely satisfactory, showing the feasibility of such device in $0.35\mu m$ technology.

Acknowledgements

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