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Design and Analysis of Amplifiers for Protective Relay Testing

Abstract. *This paper presents the analysis and design of voltage and current amplifiers for use in protective relay testing for frequencies up to the 20th harmonic. A typical topology of DC/AC 50/60Hz converters was used to achieve the nominal and peak values produced by conventional current and voltage transformers. The stability analysis is devised considering different requirements of load and frequency response for relay inputs when compared to that of a typical single-frequency power converter. The temporal response to signals with abrupt changes and multiple decaying harmonics is also investigated. Proper test signals are stored in a PC microcomputer and played-back using the analog audio output, which is conditioned to the proposed amplifier input. The amplifier's controller was implemented using a DSP with PWM and an IGBT H-bridge. Simulations and experimental results are presented for typical faults and multi-harmonic signals.*

Streszczenie. *W artykule zaprezentowano projekt i analize wzmacniacza używanego do testowania przekaźników zabezpieczających w szerokim zakresie częstotliwości, do 20 harmonicznej. Układ umożliwia także badania przy szybkich zanikach sygnału oraz przy zanikających harmonicznych. Sterownik wzmacniacza wykorzystuje układ DSP z PWM i mostkiem typu H w technologii IGBT.* ***(Projekt i analiza wzmacniacza do testowania przekaźników zabezpieczających)***

Keywords: Relay Test, Universal Power Supply, Inverter, Protective Relay
Słowa kluczowe: przekaźnik, wzmacniacz, testowanie

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Introduction

The equipment for testing protective relay currently found on the market is expensive. A relay tester uses current and voltage amplifiers to reproduce compatible signals with the requirements imposed by the relays. This entails the generation of arbitrary signals, usually in the range of DC to the twentieth harmonic with currents and voltages up to 20A and 600V respectively. Procedures for relay testing, which include a dynamic test and transient simulation tests, are presented in [1]. An interesting example found in the literature and intended for use in the educational environment was developed in [2]. However, such an environment has been described in a systemic way without the detailed design and analysis of the current and voltage amplifiers. To our knowledge, the design and analysis of such amplifiers have not yet been presented in the literature. However, commercial proprietary amplifiers are available, which are also used in RTDS (Real Time Digital Simulator) [3] [4]. A natural choice was to develop the proposed amplifiers using the class D topology that is used in many applications, including power inverters, Universal Power Supply (UPS) [5], programmable power sources [6], voltage and current control sources [7], controllers for multilevel inverters [8], etc. In these applications, the class D amplifier or inverter is used essentially to provide electric power, with a fixed-amplitude sinusoidal voltage source of 50Hz or 60Hz, which does not meet requirements for testing protective relays.

Linear amplifiers [9] would satisfy these requirements, but the class D topology commonly used in the inverter costs less, is smaller and is more efficient [10]. The signal produced by a traditional inverter, as said before, is sinusoidal 50/60Hz, and generally this is achieved using a pulse width modulation (PWM) and MOSFET or IGBT switches, followed by a second order LC filter to remove the harmonics produced by the switching frequency. These inverters are normally subjected to varying loads, which require the use of different classical techniques of control [11] as well as other more advanced techniques such as sliding mode controller [12], Deadbeat [13] and space vector PWM (SVPWM) [14].

To meet the test signal features of a relay test, an alternative would be to use a typical Audio Class D amplifier topology [15]. Where in audio applications, the signal frequencies vary between 20Hz to 20kHz, but these amplifiers have voltage and current ratings which limit their usage in relay testing. In addition, the wide bandwidth requires that audio amplifiers operate at high switching frequencies, but without necessarily using feedback on their projects . The requirements for audio amplifiers do not require the use of controllers or switching devices capable of handling high currents and voltages. As a result, the topology of a typical class D audio amplifier is not suitable for use in a relay test.

In this paper, we present the stability analysis of a controller to ensure that the class D amplifier meets the requirements of relay test. This analysis is applied to the topologies for generating the proper currents and voltages amplifiers. Simulations and experimental results are presented for typical transient signals of an electric power system, and its reproducibility is validated.

The Topology of Voltage and Current Amplifiers

Fig. 1 shows the block diagram of the proposed amplifier. The reference signal is generated by a computer and using the audio output it is sent to a digital signal processor (DSP). The analog-to-digital converter of the DSP receives this reference signal $V_r(t)$ to be sampled and used as input of the amplifier. Unlike a conventional inverter designed to operate at 50/60Hz, the proposed amplifiers must reproduce signals of the type

$$V_r(t) = \sum_{n=0}^{N} A_n e^{-\alpha_n t} cos(\omega_n t + \phi_n), \tag{1}$$

where, A_n are the amplitudes of the sinusoids, α_n the attenuation factors, ω_n and ϕ_n the frequencies and phases of the harmonic components of the reference signal. N is the number of harmonics, including the DC exponential decay $\omega_n = 0$. The reference signal is used to control an H-bridge composed of IGBT switches, through PWM. To eliminate undesired harmonic signals from of this modulation, a passive low-pass filter is used. The cutoff frequency and maximum fluctuation of current in inductors are of fundamental importance in the design of these filters. The feedback signal for the controller is obtained at the outputs of the filters. The current and voltage amplifiers are shown in Fig.2, and have a similar topology to those presented in [16]. In the case of the current amplifier, the low-pass filter is an inductor L. The

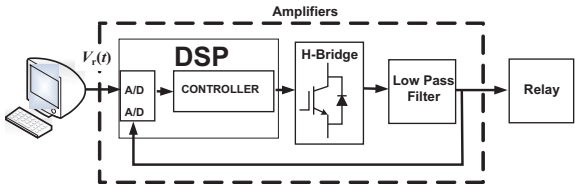

Fig. 1. Model of the proposed relay system test.

voltage amplifier has the same structure but with an output LC filter.

Analysis of Stability

Procedure project

The design of passive filter inductors depends on certain factors such as the voltage applied on the H-bridge, the size of the cross-sectional area of the core, the flux density and the maximum fluctuation of the inductor current, which decreases with increasing inductance [17]. This level of fluctuation occurs when the PWM signal is 50% of the duty cycle [16] [17]. In addition, the core material must be able to withstand the involved currents without saturating for the switching frequency [16].

The following equation was used to obtain the inductance $L = V_{DC}/(2f_{sw}\Delta i_L)$, where, f_{sw} is the switching frequency, V_{DC} is the supply voltage on the H bridge and ΔiL the maximum fluctuation of current in the inductor.

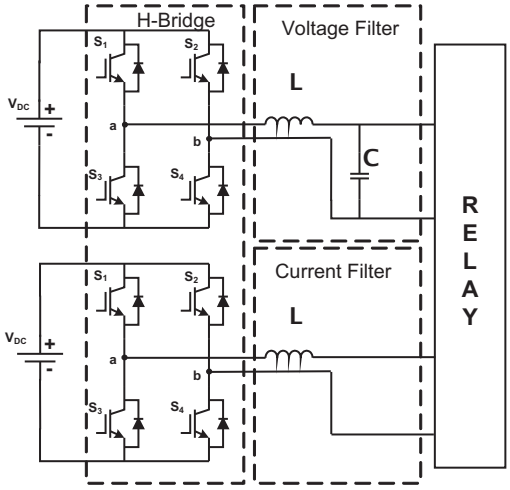

Fig. 2. Model of voltage and current amplifiers for The proposed relay system test in a monofassic configuration.

Open Loop Voltage Analysis

The topology shown at the top part of Fig. 2 was chosen to implement the voltage amplifier. The modulated signal at the bridge output passes through a low-pass LC filter. This filter would lead to instability for high impedance loads because of the resonance peak at the cutoff frequency. In this work, we added a resistance R as Fig. 3 with a low value compared to the input impedance of the relay R_s. In common inverter applications, this resonance is attenuated by a very low impedance load. However, the R value is kept as low as possible, but limited to a still high value because of the maximum dissipated power at the output. To reduce the resonance peak to a suitable value, while maintaining the R value, we propose the insertion of a $R_A L_A C_A$ trap filter tuned at the cut-off frequency and a compensation resistor R_C in series with the inductor L, as shown in Fig 3. An important feature of the trap filter is that its power consumption only occurs at the cutoff frequency, resulting in negligible power amplifier loss.

The transfer function of the voltage across the load

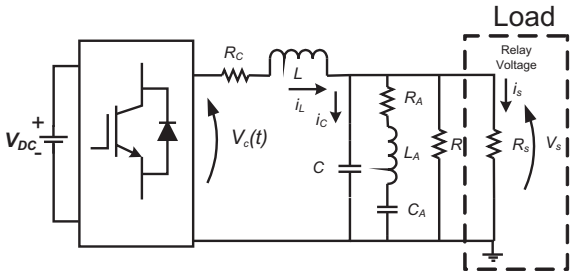

Fig. 3. Proposed Model for the Voltage Amplifier.

impedance and the IGBT bridge output is given by (2) considering $L_A = L$, $C_A = C$, $R \gg R_A$ and $Rs \gg R$. This last consideration takes into account that commercial relays may present input impedance values of over hundreds of $k\Omega$.

$$(2) \quad F_{vc}(s) = \frac{V_s(s)}{V_c(s)} = \frac{RLCs^2 + R_A RCs + R}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0},$$

Where: $b_4 = RL^2C^2$, $b_3 = LC(L + RC(R_A + R_C))$, $b_2 = C(L(3R + R_A + R_C) + R_A R_C RC)$, $b_1 = L + C(R_C(2R + R_A) + RR_A)$, $b_0 = R + R_C$

The signal $V_c(t)$ in Fig. 3 depends on the reference voltage $V_r(t)$, the supply voltage V_{DC} and the bridge switching frequency. A controller must ensure that the amplifier output follows the reference signal with minimum error. The proposed controller is designed to act on the H-bridge in order to obtain flat unit gain in the desired frequency range and a linear phase corresponding to a small constant time delay. In addition, the amplifier should respond quickly to abrupt transient inputs.

Open Loop Current Analysis

The topology of the current amplifier is shown in Fig. 4. Its output filter consists of an inductor L and a burden load resistance R_B corresponds to the input impedance of the relay. The transfer function relating the IGBT bridge output voltage and the load current is given by.

$$(3) \quad F_{iL}(s) = \frac{i_{RB}(s)}{V_c(s)} = \frac{1}{LR_B},$$

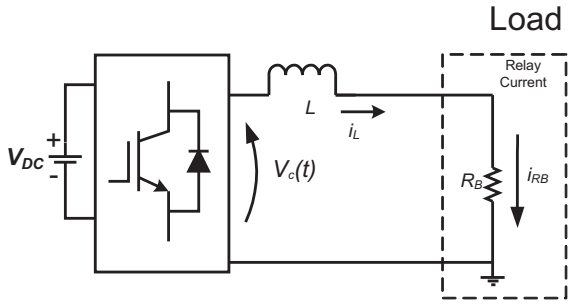

Fig. 4. Topology of the current output filter amplifier.

The analysis of the transfer function described by equation (3) shows that for commercial burdens R_B varying between $0.1 - 1\Omega$ causes undesired large variations in magnitude and phase response. Thus, it is necessary to insert a current amplifier controller to ensure the desired response.

Closed Loop Voltage Amplifier Analysis

The proposed controller for the voltage amplifier is presented in Fig. 5. It is a parallel combination of the closed loop controller $C_v(s)$ with a feedforward controller $H_1(s)$, this with transfer function of a low pass filter with cutoff of 3kHz. The

large difference between the sampling rate (20kHz) and the maximum signal frequency (1.2kHz) makes the amplifier response sensitive to the zero order hold (ZOH), which represents the PWM digital-to-analog converter at the DSP output. The function that describes the ZOH is the term that multiplies $F_{vc}(s)$ in the equation (6) and $F_{vc}(s)$ is the mathematical representation of the low pass filter described by the equation (2). The computational delay effect described and discussed in [18] [19] [20] is neglected because we use a high-speed DSP with interrupt management at sampling times.

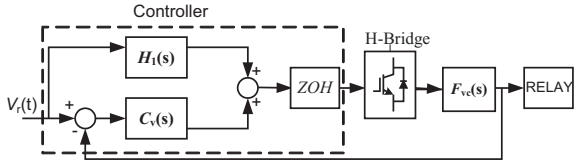

Fig. 5. Block diagram of the of the voltage amplifier controller.

The transfer function of the complete controller, shown in Fig. 5, is given by

$$\frac{V_s(s)}{V_r(s)} = \frac{F_{vc}(s)ZOH(s)[H_1(s) + C_v(s)]V_{DC}}{1 + C_v(s)ZOH(s)F_{vc}(s)}, \quad (4)$$

The controller $C_v(s)$ complements the control action of $H_1(s)$, using a block proportional-integral with a cascaded phase lead compensator, given by

$$C_v(s) = (10 + \frac{120}{s})(\frac{s + 2\pi 3000}{s + 2\pi 30000}), \quad (5)$$

The zero-order hold is incorporated into the output analog filter as

$$F_v(s) = \frac{1 - e^{-Ts}}{sT} F_{vc}(s), \quad (6)$$

As the controllers are embedded in a DSP, the stability system analysis has to be carried out in discrete time. Therefore, the filter $F_v(s)$ and the controller $C_v(s)$ are mapped to the Z domain as expressed by equations (7) and (8) respectively.

$$F_v(z) = Z[F_v(s)] = (1 - z^{-1})Z[\frac{F_{vc}(s)}{s}], \quad (7)$$

$$C_v(z) = C_v(s)|_{s=\frac{2}{T}\frac{z-1}{z+1}}, \quad (8)$$

The stability analysis of the proposed system can be performed using traditional techniques such, phase and gain margins analysis and the Roots-Locus method (LGR) [21][22]. In the present work, the stability of the system for different input resistances or loads in the amplifier output must be guaranteed. Thus, we chose the LGR method for our analysis because the other method only allows us to verify if the system is marginally stable. It should be noted that the LGR technique used here does not use the gain variation, as in the traditional method. Alternatively, the open loop gain of the system (4) is regarded as unitary, and the load resistance R varies within a range of interest. Fig. 6 shows the stability of system for variations in the load resistance from 1Ω to $10k\Omega$. However, it is important to remember that low values of load resistances result in excessive and unnecessary power dissipation. Therefore, this limitation should be taken into consideration during the design of the amplifier. Fig. 7 shows the frequency response of the closed-loop voltage amplifier $V_s(s)/V_r(s)$ for a load resistance of $10k\Omega$. The resulting response is flat in magnitude in the desired band, with

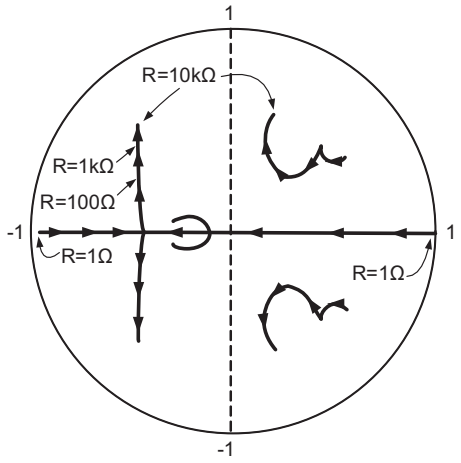

Fig. 6. LGR of the controller $C_v(z)F_v(z)$ with an load resistance R variable in the range of 1Ω to $10k\Omega$.

low harmonic distortion in the signal to be amplified. However, this controller does not provide a flat phase response at high frequencies. Despite this, you can playback most typical fault signals of an electrical system without relevant loss for a relay test.

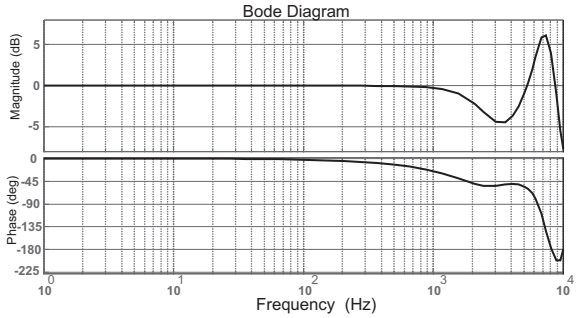

Fig. 7. Frequency response of the closed-loop voltage amplifier for R = $10k\Omega$.

Closed-Loop Current Amplifier Analysis

The current amplifier is designed using a similar procedure to that of the voltage amplifier. The modeling of this amplifier is represented by (9) with $F_{iL}(s)$ provided by the equation (3).

$$F_i(s) = \frac{1 - e^{-Ts}}{s} F_{iL}(s), \quad (9)$$

To ensure a flat magnitude response, with minimal phase lag, we designed a proportional-integral controller in cascade with a compensator as described in (10).

$$C_i(s) = (10 + \frac{10000}{s})(\frac{s + 2\pi 3500}{s + 2\pi 3200}), \quad (10)$$

The stability analysis of the current amplifier is made in the discrete domain. Thus, $F_i(s)$ and $C_i(s)$ must be mapped to this domain, as shown in the equations (11) and (12).

$$F_i(z) = Z[F_i(s)] = (1 - z^{-1})Z[\frac{F_{iL}(s)}{s}], \quad (11)$$

$$C_i(z) = C_i(s)|_{s=\frac{2}{T}\frac{z-1}{z+1}}, \quad (12)$$

Fig. 8 shows the LGR analysis of the system $C_i(z)F_i(z)$ for typical relay burden commercial values [3]. It can be observed that the stability is maintained for the entire range of load resistance. The closed-loop frequency response for

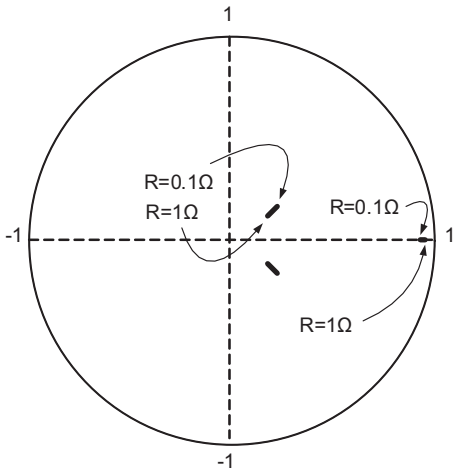

Fig. 8. LGR of the controller $C_i(z)F_i(z)$ with a load resistence R_B variable in the range of 0.1 - 1Ω.

$R_B = 1\Omega$ can be observed in Fig. 9. In this case, the magnitude is flat with a variation of less than 0.5 dB at a range of 100Hz to 1.2kHz. The phase response behaves similar to that of the voltage amplifier, with similar implications in the reproduction of fault signals.

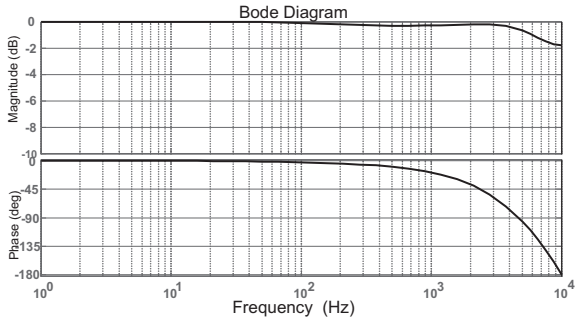

Fig. 9. Frequency response of the closed loop $C_i(z)F_i(z)$ current amplifier for R_B of 1Ω.

Results

Simulation Results

Transient signals representing typical electrical system faults are generated by simulation and played back in an experimental prototype to test the performance of the amplifiers. These signals contain spectral components as described in equation (1). Table I shows the component values and parameters used in the simulation and experimental results.

Table 1. Values of Components and Parameters of the Amplifiers

Description	Symbol	Value
Filter Capacitance	C	$2.8\mu F$
Filter Inductance Voltage	L	$1mH$
Filter Inductance Current	L	$500\mu H$
Switching Frequency	f_{sw}	20kHz
Network Frequency	f_0	$DC - 20^a harmonic$
Supply voltage	V_{DC}	200V
Damping Resistor	R_D	10Ω
Filter Resistor	R_A	20Ω

The simulation shown in Fig. 10 illustrates the effect of an overcurrent fault in the feeder voltage, which immediately decreases during the occurrence. The reference signal sent to the voltage amplifier was simulated for a single phase network. It can be noted that the controller is capable of reproducing the reference (see detail) in less than 1ms. Fig. 11 shows the simulation of a transient current for a fundamental of 60Hz and an exponentially decaying DC component with a harmonic of 1.2 kHz. The amplifier follows the reference signal introducing a phase delay in the twentieth harmonic, according to the frequency response shown in Fig. 9.

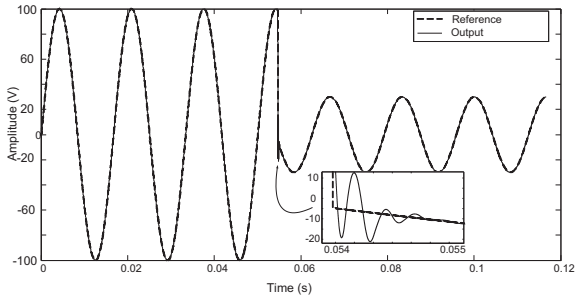

Fig. 10. The reference signal and its corresponding voltage response at the amplifier output for an overcurrent condition.

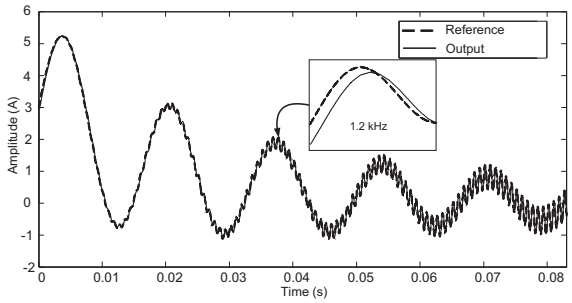

Fig. 11. Simulation of a transient current signal with exponentially decaying DC component and increasing harmonic of 1.2 kHz.

Experimental Results

The experimental prototype is shown in Fig. 12. It is uses an IGBT H-bridge three-phase model IRAMX20UP60A, which supports maximum voltages of 600V and currents up to 20A. The maximum switching frequency of the bridge is 20kHz and this is used as the sampling frequency of the control algorithm. The LC filter is built with a ferrite core and multi-wire winding, and it responds to the twentieth harmonic with negligible losses. The current sensor used is the LEM LA55P and the voltage sensor is the LV20-P. The digital controllers are embedded in a Texas DSP TMS320F28335. The program MATLAB is used to generate electrical faults and the analog audio output of the computer is used to generate the references, this output is conditioned to the proposed class D amplifier input. Figs. 13 and 14 show the experimental results corresponding to the simulation presented in Figs. 10 and 11, respectively.

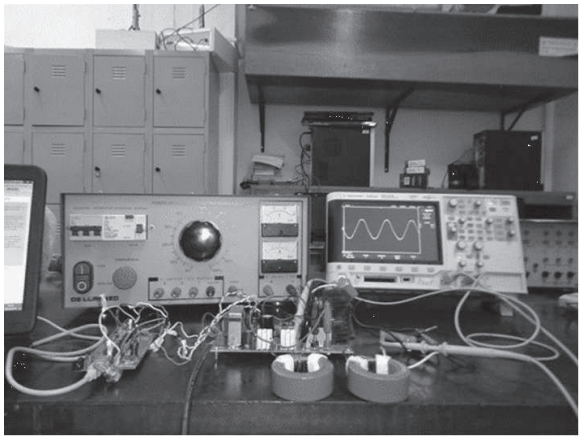

Fig. 12. Experimental prototype.

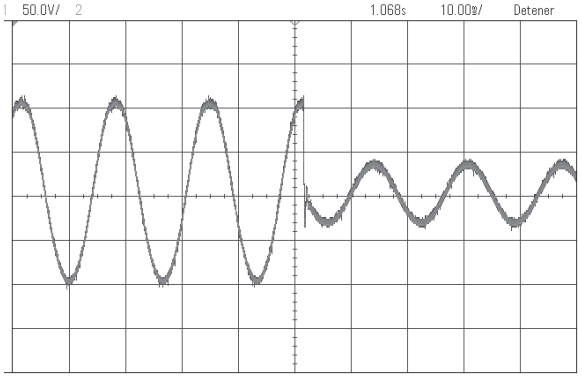

Fig. 13. Experimental result voltage response at the amplifier output for an overcurrent condition.

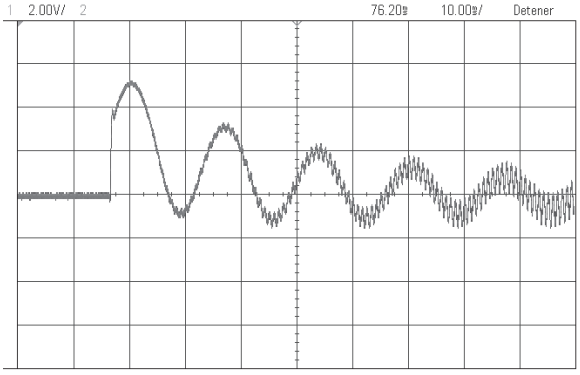

Fig. 14. Experimental result of a transient current signal with exponentially decaying DC component and increasing harmonic of 1.2 kHz.

Conclusion

The design of current and voltage amplifiers for use in protective relay test has been described. The analysis of a feedback stability of the amplifiers was presented describing curves for load variations where the amplifiers can be unstable. The control method used to guarantee the stability analysis was the root locus, where the entire amplifier model were mapped in the Z domain. In addition, the procedure to calculate the passive elements of the power amplifiers such as inductance and capacitance of the filter was described. A frequency analysis of these amplifiers was performed to ensure a flat magnitude response and minimal phase delay. The amplifiers were simulated and tested experimentally for some types of transient signals, composed of harmonics, abrupt changes and exponential decays. The good performance obtained in simulation was verified experimentally, in both frequency and time domain. The results show that the proposed amplifiers may be used for relay testing in the range of DC to 1.2 kHz.

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