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# High efficiency isolated DC/DC boost converter with planar magnetics for photovoltaic applications

***Abstract***. *Classic high-frequency transformers enable for isolated DC/DC converters to achieve high input voltage gain by the turns ratio. Through the use of an isolation transformer made in planar technology with interleaved windings leakage inductance can be significantly reduced and voltage overshoots can be marginalized. By applying balancing transformer with integrated input inductor in the setup of the converter current flowing through the semiconductor switches can be decreased and their conduction losses could be reduced. Additionally integrating input inductor with balancing transformer by core sharing helps to reduce number of magnetic components in the circuit. In this paper laboratory measure results as well as theoretical analysis of the half-bridge step-up DC/DC converter with planar transformer and integrated input inductor are presented. The test system achieved a 12-fold voltage gain and efficiency over 95%.*

***Streszczenie.*** *W izolowanych przekształtnikach DC/DC, dzięki odpowiedniej przekładni tradycyjnego transformatora wysokiej częstotliwości, osiągamy znaczne wzmocnienie napięcia wejściowego. Skutkiem użycia planarnego transformatora izolującego z sekcjonowanymi uzwojeniami było znaczne zmniejszenie indukcyjności rozproszenia transformatora i przepięć na tranzystorach. Zastosowanie w przekształtniku planarnego transformatora wyrównawczego spowodowało zmniejszenie prądów i strat przewodzenia w łącznikach. Zredukowano gabaryty i liczbę elementów magnetycznych poprzez zespolenie dławika wejściowego z transformatorem wyrównawczym na jednym rdzeniu magnetycznym. W pracy przedstawiono analizę teoretyczną oraz wyniki badań laboratoryjnych półmostkowego przekształtnika podwyższającego DC/DC z planarnym transformatorem wyrównawczym zintegrowanym z dławikiem wejściowym. Badany układ osiągnął 12-krotne wzmocnienie napięcia i sprawność powyżej 95%. (**Wysokosprawny izolowany przekształtnik podwyższający DC/DC z transformatorami planarnymi do zastosowań w fotowoltaice**).*

**Keywords**: high efficiency, boost DC/DC converter, integrated planar transformer, photovoltaic systems.
**Słowa kluczowe** wysoka sprawność, przekształtnik podwyższający DC/D, planarny transformator wyrównawczy, systemy fotowoltaiczne.

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## Introduction

In many applications with low input DC voltage considerably larger output voltage is needed. Such applications include fuel cells and photovoltaic (PV), where the voltage obtained is low (generally tens of volts). Individual solar cells can be connected in series and/or in parallel. In order to maximize the power generation from each cell corresponding to its particular irradiance level the best choice is the parallel connection [1]. This solution has the advantage over panels connection in series because the least efficient panel does not determine the current of the whole system.

The parallel configured solar energy systems are composed of PV arrays, DC/DC boost converter and DC/AC inverter. With the efficiency achieved by the commercially available PV panels rarely exceeding over a dozen of percent, it is very important that the efficiency of the DC/DC converter is as high as possible. The step-up DC/DC power converter is attached to boost PV panel terminal voltage, since parallel-configured solar array provides voltage generally too low to be directly utilized by most applications. In order to obtain voltage level needed for direct to alternating current conversion the DC/DC power converter should demonstrate significant voltage gain. To obtain such level of output voltage at low input voltages, transistors of the boost converter must operate with high currents. Large DC input currents cause an increase in power losses as the transistor conduction losses are proportional to square of current. The solution to this problem would be to divide a large input current into smaller currents through applying coupled inductors or balancing transformers [2]-[7] in converter structure. Integration input inductor with balancing transformer by core sharing helps to reduce number of magnetic components in the circuit.

The converter topology presented in this paper suits for an application where low voltage high current source such as string of photovoltaic panels supplies DC/DC power stage. Detailed operation, analysis, design and experimental results for the converter are presented.

## Electrical scheme

The proposed DC/DC converter is shown in Fig. 1. The DC/AC and AC/DC power stages are separated through transformer $T_2$ (turns ratio 1:$n$, where $n$=2). The converter is supplied from constant DC source which with integrated input inductor $L_1$ form constant current source. Balancing transformer $T_1$ ensures equal distribution of input current $i_{\text{in}}$. The MOSFET-type transistors form input half-bridge they are conducting alternatively or together according to driving time period. The transformer $T_2$ provides galvanic isolation and multiplies ($n$) half-bridge output voltage. The secondary side of isolation transformer is connected to rectifier half bridge consisting of diodes $D_1$, $D_2$ and voltage doubler capacitors $C_1$, $C_2$.

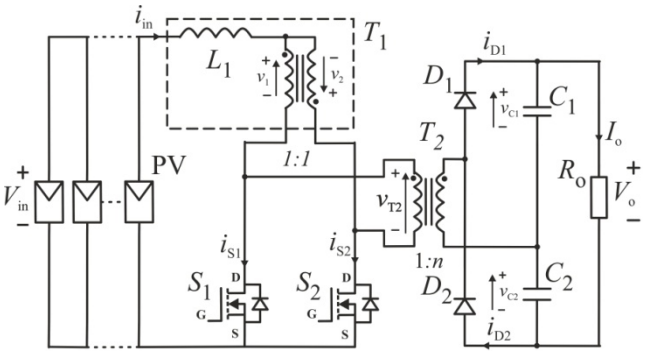


Fig. 1. Isolated half-bridge DC/DC boost converter with planar transformers and integrated input inductor

The main advantages of the converter are: a) high efficiency despite of hard transistor switching; b) high voltage gain; c) small number of semiconductors; d) modular and simple design. The output across the half bridge converter can be managed via duty cycle *D* of semiconductor switches $S_1$ and $S_2$.

**Planar Magnetics**

In many converter topologies implementation of planar magnetic was considered [8]. The planar transformers current density flowing through the windings is greater than that of the circular section. As a result, the efficiency of the planar transformer can be much higher than the transformer made in a traditional way, and this at much smaller sizes. Additionally by interleaving of the planar transformer windings leakage inductance can be significantly reduced.

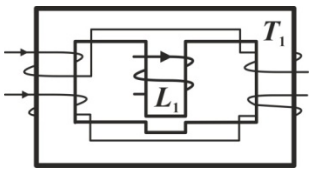


Fig. 2. Pictorial diagram of Inductor $L_1$ and a transformer $T_1$ integrated into a single core

To meet the requirement for low profile and high power density in step-up converter applications, integrated magnetic are investigated in the past years. Transformers and inductors can be constructed in one magnetic core by sharing a common magnetic path. In this way, the number of magnetic cores is reduced, and the flux ripple may be suppressed. The most important feature of integrated magnetic in low voltage high current applications is minimization of interconnects which helps to increase the efficiency of power electronic converter.

**Analysis of operation**

The key steady state waveforms of the proposed converter are shown in Fig. 2. There are four control subintervals, however and only two of them are analyzed in detail because the other two are similar.

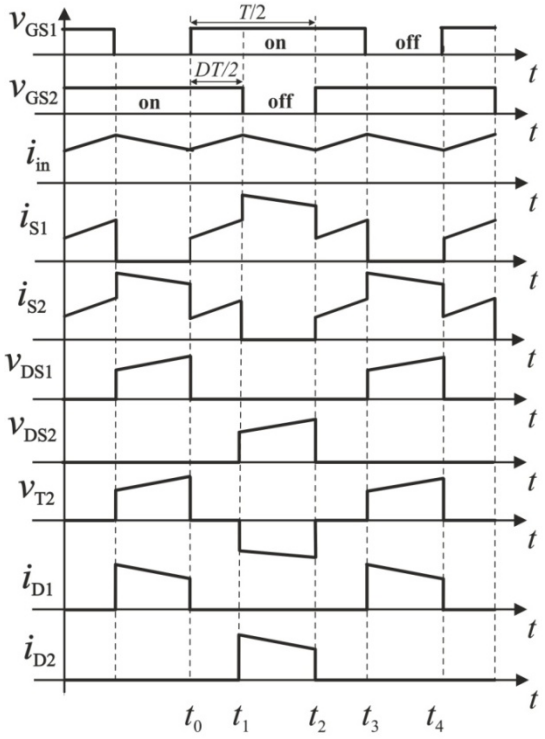


Fig. 3.Theoretical waveforms of isolated DC/DC boost converter with planar transformers and integrated input inductor

As can be seen from the timing diagrams in Fig. 2 during ($t_0$-$t_1$) switches $S_1$ and $S_2$ conduct with overlapped control signals. The time of simultaneous conduction begins when one of the switches is turned-on and another transistor starts to conduct. This time represents $DT/2$ control period of the converter. Since the both switches are in on state input voltage $V_{in}$ is

$$V_{in} = v_1 + L_1 \frac{di_{in}}{dt} \tag{1}$$

Where $v_1$ is voltage on transformer $T_1$ primary winding. Since the turns ratio of the $T_1$ transformer is 1:1, input current is always divided equally

$$v_1 + L_1 \frac{di_{in}}{dt} = -v_2 + L_1 \frac{di_{in}}{dt} \tag{2}$$

and have the same rate of change in both transistor branches $v$=$v_1$=$v_2$. If the transformer $T_1$ secondary and primary inductances have the same value

$$\frac{di_{in}}{dt} = \frac{V_{in} - v}{L_1} = \frac{V_{in} + v}{L_1} \tag{3}$$

we can assume that $v_1$ = -$v_2$ => $v$ = 0. Therefore,

$$\frac{di_{in}}{dt} = \frac{V_{in}}{L_1} \tag{4}$$

.

As the output is decoupled from input voltage output diodes $D_1$ and $D_2$ are turned off. During this time interval load is supplied from output capacitors $C_1$ and $C_2$.

Switch $S_2$ is turned off at ($t_1$) transistor $S_1$ starts to conduct all the input current $i_{in.}$ During ($t_1$-$t_2$) diode $D_2$ is forward biased and conducts transformer secondary current. The input current decreases and the voltage across both balancing transformer windings $v$ is equal to voltage on capacitor $C_2$ including the transformers $T_2$ turns ratio

$$v = \frac{v_{C2}}{n} \tag{5}$$

.

Assuming that inductances of both balancing transformer windings are equal

$$\frac{di_{in}}{dt} = \frac{V_{in} - v}{L_1} = \frac{1}{L_1}(V_{in} - \frac{v_{C2}}{n}) = \frac{1}{L_1}(V_{in} - \frac{v_C}{n}) \tag{6}$$

Where $v_C$= $v_{C1}$= $v_{C2}$. Current charges capacitor $C_2$, capacitor $C_1$ continues to be discharged by the load current $I_o$.

At ($t_2$) switch $S_2$ is turned on. This begins ($t_2$-$t_3$) time interval which is identical to ($t_0$-$t_1$). During this stage both switches are on and input current increases. Output rectifiers are reverse biased. Input and output power stages are decoupled from each other. At ($t_3$) transistor $S_1$ is turned off the $S_2$ is conducting all the input current $i_{in}$. The driving cycle ends with time period ($t_3$-$t_4$) which is similar to ($t_1$-$t_2$) Capacitor $C_1$ is charged by transformer $T_2$ secondary winding current capacitor $C_2$ is discharged by the load.

The voltage gain ratio can be calculated form volt-second balance equation

$$\frac{V_{in}}{L_1} D\frac{T}{2} = \frac{(V_{in} - \frac{v_C}{n})}{L_1}(\frac{T}{2} - D\frac{T}{2}) \tag{7}$$

Summary voltage of both voltage doubler capacitors $C_1$, $C_2$ can be described as

(8) $$2v_C = V_o .$$

Considering equations (7) and (8) voltage gain ratio $B$ is given by

(7) $$B = \frac{V_o}{V_{in}} = \frac{2n}{(1-D)}$$

It should be noted, that this type of converters must operate with duty cycle $D$ above 0.5. Bearing in mind that transformer turns ratio is $n$=2, minimum voltage gain achieved in the system is 8.

**Experimental Verification**

The proposed converter has been designed with rated output power 1.5 kW (maximum 1.8 kW) at input voltage $V_{in}$ varied from 10 V to 50 V. Low-voltage power source was simulated by MAGNA-POWER ELECTRONICS XR-50-100 power supply.

Driving signals were generated in Cyclone III FPGA. Both transistors had optically isolated driving circuitry followed by MOSFET transistor driver and the gate driving network to optimize turn off time of the transistors. The switching frequency $f_S$ of the converter was 19.53 kHz. Since the semiconductors of the converter were hard switched and the driving frequency was relatively low the conduction losses dominated in this design. In order to keep energy losses as low as possible MOSFET transistors used in this design had 2 mΩ drain to source resistance. In order to reduce switching losses of output rectifier silicon carbide diodes were used. They do not suffer from reverse recovery so their turn off losses could be omitted. Table 1 lists the components used in the construction of the converter.

Table 1. Half-bridge isolated converter components

| Component | Type | Specification |
|---|---|---|
| Power transistor $S_1$,$S_2$ | IRFP4468 | 2 mΩ /100 V |
| Output diode $D_1$,$D_2$ | SDT12S60 | 12 A /600 V |
| Input inductor $L_1$ | integrated | 12 uH /40 A |
| Balancing transformer $T_1$ | T1000DC | Turns ratio 1 |
| Isolation transformer $T_2$ | T250DC | Turns ratio 2 |
| Output capacitor $C_1$,$C_2$ | PCW245 | 30 μF/700 V |

Measurements of transient characteristics of the converter were made using the Tektronix DPO5034 oscilloscope Efficiency and input/output parameters measurements were made using the HIOKI 3390 power analyzer. All of the voltage and current probes used in these devices were properly calibrated.

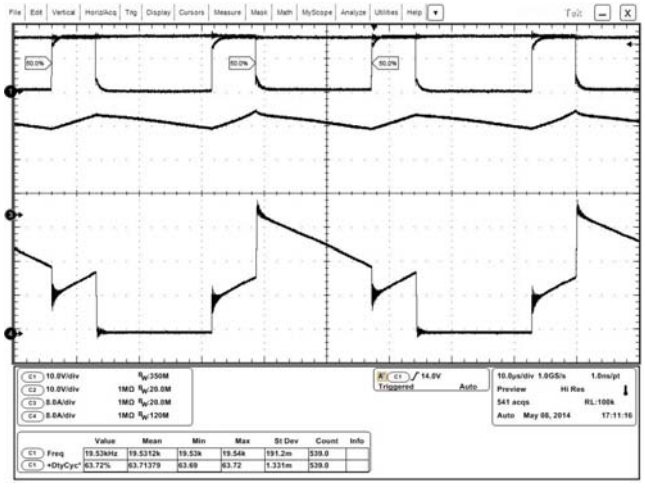

Fig.4. Measured waveforms of ch1,2-driving gate signals $v_{GS1}$, $v_{GS2}$, ch3-input current $i_{in}$, ch4-transistor $S_1$ current $i_{S1}$

In Figure 4 and Figure 5 transient characteristics of the converter for 440 W input power and 0.64 duty cycle can be seen. Voltage spikes across transistor seen in Fig. 5 are disadvantageous phenomenon and will contribute to the turn-off losses of the transistors but they are in the range of transistors rated voltage. This oscillation is mainly caused by leakage inductance of isolation $T_2$ transformer. The same parasitic voltage overshoots are present in primary side transformer voltage $v_{T2}$.

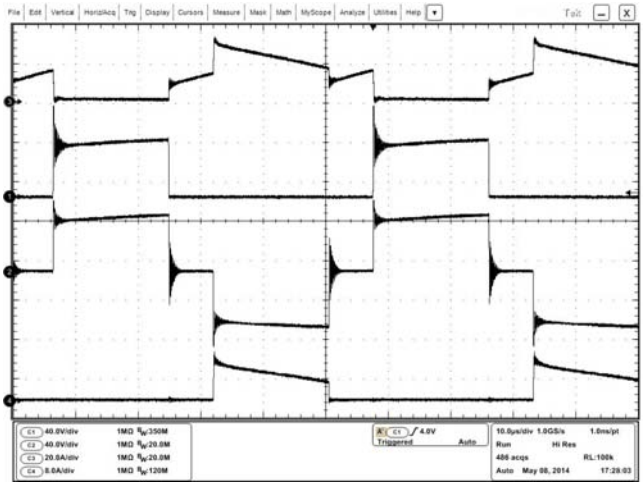

Fig.5. Measured waveforms of ch1-transistor $S_1$ current $i_{S1}$, ch2-transistor $S_1$ drain-to-source voltage $v_{DS1}$, ch3-transformer $T_2$ primary side voltage $v_{T2}$, ch4-diode $D_2$ current $i_{D2}$

Waveforms presented in Figure 6 show measured input and output voltage of the converter for duty cycle 0.54 and input power ~1.1 kW. For approximately 40 V of input voltage ~340 V output was achieved indicating 8.5 voltage gain. Output current for this operation point was 3.28 A. Maximum transistor voltage overshoot was 21.59 V. Measured waveforms reflected theoretical assumptions.

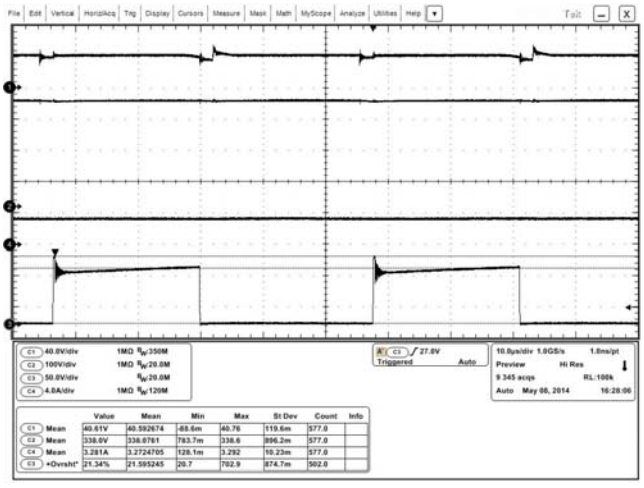

Fig.6. Measured waveforms of ch1-input voltage $V_{in}$, ch2- output voltage $V_o$, ch3- transistor $S_1$ drain-to-source voltage $v_{DS1}$ , ch4-output current $I_o$

The specific data points for efficiency curves were acquired from HIOKI 3390 power analyzer. In Figure 7 an example operating point of the converter can be seen. Substantial is the difference between input and output voltages and currents. In spite of the large differences between them energy losses in the system are minor.

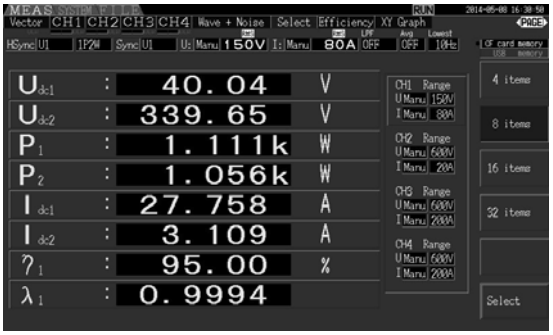


Fig. 7. An example of the operating point of the converter

Maximum measured converter efficiency was 95.86% for 30 V input voltage and 628 W of processed power. As can be seen in Fig. 8 converter maintain efficiency over 91,7% for all power range and for the scope of 350 W to 1200 W the converter efficiency was above 94% despite hard switching of semiconductors.

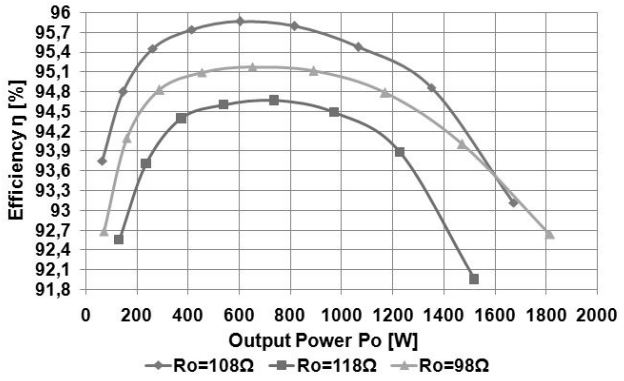


Fig.8. Efficiency $\eta$ versus output power $P_o$ for three different output resistances $R_o$=98 Ω, 108 Ω , 118 Ω for different input voltages from 10 V to 50 V

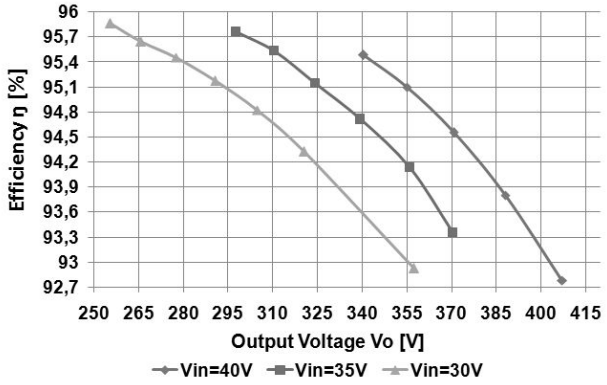


Fig.9. Efficiency $\eta$ versus output voltage $V_o$ for three different input voltages $V_{in}$=30 V, 35 V, 40 V for different duty cycle *D* from 0.54 to 0.68

Figure 8 presents results from three test measurements of the converter output voltage and efficiency for three different input voltages from the range that strings of parallel solar panels usually provide. The converter achieved output voltage over 330 V for all input voltages with maintain the efficiency over 93.5%. So even at adverse supply condition converter preserves it's functionality.

**Conclusion**

A high voltage step-up isolated half-bridge DC/DC converter for low input high current applications has been proposed in this paper. It is composed of the DC/AC half-bridge boost converter with balancing transformer and integrated input inductor connected via isolation transformer with half-bridge rectifier and voltage doubler. The high frequency planar transformers used in the converter contribute to lowering energy losses in the system. The performance of the converter has been studied with several test measurements in different supply and load conditions. Prototype converter has been designed with 19.53 kHz switching frequency and 1.5 kW rated power. The converter peak efficiency was 95.86% despite the fact that all semiconductors in the circuit were hard switched. The higher voltage gain reported was 12. Therefore, the designed converter is suitable for low input voltage photovoltaic systems requiring high voltage gain and high efficiency.

By applying planar isolation transformer with interleaved windings leakage inductance can be significantly reduced and voltage overshoots can be marginalized. Unfortunately, they have not been eliminated completely as can be seen in transistor voltage waveforms. It is noteworthy that for the higher input power the parasitic overshoots percentage contribution to the maximum transistor voltage decreases.

In order to further efficiency increase transistor soft switching techniques could be applied.

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