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Adaptive Frequency Compensation in Amplifiers for Protective Relay Testing

Abstract. *In a previous work, we presented an analysis and design of voltage and current amplifiers for use in protective relay testing for frequencies up to the 20^{th} harmonic. Beyond this limit, undesired phase and magnitude deviations occur due to the sampling rate, which defines the working frequency range of the amplifiers. To obtain a broader range of protective types of testing is desirable higher signal frequencies. For the current state-of-art of the output IGBT H-bridge, it is not possible to increase the sampling rate. In the present paper, we propose frequency compensation using an LMS-based adaptive FIR filter between the controller and the reference signal, to correct the amplitude and phase distortions. Theoretical and numerical investigations indicate the proposed method can extend the working range, up to the 50^{th} harmonic.*

Streszczenie. *W poprzedniej pracy analizowano wzmacniacze używane do testowania przekaźników zabezpieczających z zakresem częstotliwości do 20 harmonicznej. W artykule zaproponowano metodę kompensacji częstotliwości wykorzystującą filtr adaptacyjny umieszczony między sterownikiem a sygnałem odniesienia w celu korekcji zniekształceń amplitudy i fazy. Udało się w ten sposób rozszerzyć zakres częstotliwości do 50 harmonicznej.**(Adaptacyjna kompensacja częstotliwości we wzmacniaczu używanym do badania przekaźników zabezpieczających)***

Keywords: Adaptive LMS, FIR filter, Relay Test, Protective Test
Słowa kluczowe: filtry adaptacyjne, badania przekaźników, filtry SOI

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Introduction

Protective relays are employed in distribution, transmission and generation of electrical energy, as well as in industrial plants. To deal with these devices, commissioning engineers are responsible for creating and carrying out test procedures, ensuring that operational equipment work to their specification, avoiding damages and blackouts. Universal testing equipment are available in the market nowadays intended for all types of traditional protective relays [1-3]. They come with a pre-programmed typical set of tests, which usually satisfies most field demands. These commercial test equipment are not an option for senior engineers when diagnosing more complex network problems, or a researcher investigating and developing new fault detection algorithms. Therefore, some manufacturers offer proprietary PC-controlled testing systems with software modules optimized for unique functions. These are more flexible than conventional field equipment; nevertheless they are still proprietary and also expensive closed solutions. For flexible and more advanced applications, a system usually referred to as RTDS (Real Time Digital Simulator) [4] is commercially available at prohibitive costs for many research groups, educational purpose, and small manufacturer companies of relays and other control equipment.

No matter being a conventional or PC-controlled test equipment, even a state-of-art RTDS, they all need power amplifiers to emulate the voltage and current transformers ratings, originally designed to drive high-burden electromechanical relays with high power demands TP and TC[5]. These amplifiers also need to meet required: frequency bandwidth; both voltage and current maximum ratings; and the wide range of burdens, from the first generation of analog electronic relays to the latest IEC 61850 IEDs (Intelligent Electronic Devices) [6,7]. For PC-controlled equipment, test procedures include stead-state and transient signals obtained from a digital fault recorder or a simulation program, such as EMTP (Electromagnetic Transients Program) or MATLAB. The signals may be recorded as COMTRADE (Common Format for Transient Data Exchange) or WAV files and can be played back using digital-to-analog converters or PC audio outputs. These both voltage and current signals are amplified and then connected to corresponding relay inputs.

In a recent paper [8] we proposed and presented the design and analysis of such types of amplifiers. The obtained experimental results adequately reproduce test signals limited to the 20^{th} harmonic. Other possible design choice to extend the working frequency would be the use of typical class-D audio amplifier topologies [9,10]. In these amplifiers, arbitrary signals in the frequency range of 20Hz to 20kHz can be reproducible at moderate voltage output levels. This characteristic is incompatible with relay test amplifiers, since they need around 600V output peak voltage to correctly emulate a potential transformer during a fault. Most types of audio amplifier require high switching frequencies to reproduce a 20kHz audio signal [11]. These switching frequencies are unsuited with the slew-rate and voltage-current peaks of the IGBT switching device needed to achieve the ratings of relay amplifiers. In addition, due to a psychoacoustic phenomenon, only harmonic distortion matters for audio amplifiers, since neither group nor phase delays [11] up to some levels are perceptible to most human beings. Thus, audio design is much concerned with low harmonic distortion [10], which leads to very specific circuit topologies and control strategies [9-11]. On the contrary, digital relays and their algorithms may be quite sensitive to phase or group delays, depending on the harmonics of interest.

In the present article, we propose a method to extend the working frequency up to the 50^{th} harmonic, which allows a broader and more flexible range of protective relay testing. For this purpose, we employ a compensation FIR (Finite Impulse Response) filter that modifies the reference signal applied to the amplifier input, to mitigate its magnitude and phase distortions, producing the desired frequency compensation. Using the amplifier model obtained in the previous work [8], we introduce some modifications including the discretization of external analog filter components. With a novel proposed controller, the FIR filter coefficients are estimated using an LMS (Least Mean Square) algorithm for each signal to be played back. The following sections present a study of the proposed topology, FIR compensator and LMS implementation. The data from simulations, showing the potential effectiveness of the proposed technique are presented at the results section.

Topologies of voltage and current amplifiers

In the previous paper [8] the output analog filter of the voltage amplifier has employed a damping trap circuit to keep the system with a fast response, while maintaining the stability. To reduce the use of external electrical components, we propose an internal digital filter to emulate the same effect of the external one. The topology proposed for the voltage amplifier is simplified and presented in Fig. 1. We maintain the resistance R with a low value compared to the input impedance of the relay R_s. Fig. 2 shows the analog version $F(s)$ of the digital filter $F(z)$ transfer function, to be incorporated into the controller $C(z)$. We keep the same $R_A L_A C_A$ trap filter tuned at the cut-off frequency with a compensation resistor R_c. The capacitor C_d with a small value is added to keep the stability of the digital version of $F(z)$, obtained using bilinear transformation. The continuous version of the filter transfer function is given by

$$F(s) = \frac{V_{of}}{V_{if}} = \frac{L_A C_A s^2 + C_A R_A s + 1}{as^3 + bs^2 + cs + 1}, \quad (1)$$

where
$a = C_d L_A C_A R_c$
$b = L_A C_A + R_c R_A C_d C_A$
$c = R_c C_A + R_c C_d + C_A R_A$
The new controller is a function of $F(s)$ in cascade with a PI controller given as:

$$C(s) = (k_p + \frac{k_i}{s})(\frac{2\pi f}{s + 2\pi f})F(s), \quad (2)$$

$$C(z) = C(s)|_{s=\frac{2}{T}\frac{z-1}{z+1}}, \quad (3)$$

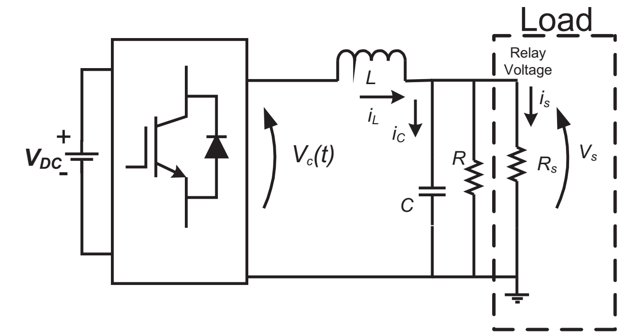

Fig. 1. Class D voltage amplifier model without damping filter.

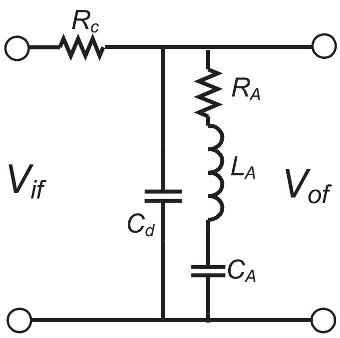

Fig. 2. Equivalent circuit for the digital trap filter $F(z)$.

Fig. 3 shows a general block diagram of the proposed amplifiers. At first glance, it seems odd to present such a diagram before introducing all of its parts. However, it will progressively become more instructive to the proper understanding of the analysis details. The amplifier was implemented using a digital signal processor (DSP) for the digital block. The analog block is an IGBT H-bridge followed by an analog output filter. The digital block is composed of floating and fixed-point structures in the discrete-time domain. It is connected to the continuous-time domain in the analog block through a zero-order hold. The input reference is the desired discrete-time signal to be reproducible at the filter output. This filter output signal is quantized to discrete-time using other ADC input, with a sampling frequency M times higher than the natural processing frequency f_s.

Any discrete-time linear dynamical system like $C(z)$ has the premise of synchronized ideal samplers at both input and output; and the calculation time T_d is assumed to be zero. When the sampling period T is much longer than the T_d, required in a practical implementation, the z-transform domain remains unchanged. On the other hand, when the T_d is on the same order of magnitude of T, the analysis should include the z-domain version of the nonlinear element e^{-sT_d}, representing a pure delay. As we can see in Fig. 3 that there is a block to represent a pure delay T_d followed by a decimation block, which resample the output filter signal at a rate M times slower than the corresponding ADC input sample rate. The controller $C(z)$ calculation time need to be $T_d = T/M$, which is obtained by the decimation in the downsampling process. Fig. 4 shows that at the beginning of a new pulse-width modulation (PWM) cycle all calculations of the sample n must be concluded, and the PWM comparison register updated. The less computational time needed for calculations, the smaller may be the delay or higher the sample frequency Mf_s. For the present amplifier, the maximum switching frequency of the IGBT bridge is the sampling frequency $f_s = 1/T = 20kHz$. A second nonlinear element, the zero-order hold or PWM ZOH, represents the PWM comparison register, which holds during the whole period T, producing the corresponding average value at the PWM output. For low frequencies as 50Hz or 60 Hz, the ZOH magnitude and phase responses have very small effects on the precise reproducibility of the reference signal and its frequency response is mostly neglected in power electronics applications. However, as a reference signal frequency increases, the dynamic response of the ZOH has significant effects and needs to be taken into consideration in the controller analysis. Finally, the analog filter $G(s)$ is responsible for the PWM averaging and suppression of high-frequency spectral components. Its transfer function, including the relay voltage load is given by:

$$G(s) = \frac{\frac{1}{LC}}{s^2 + \frac{s}{RC} + \frac{1}{LC}}, \quad (4)$$

where L and C are values of the passive filter LC. Relay testing amplifiers should have the capacity to reproduce not only a single-frequency signal, as most inverters do, but also band-limited arbitrary signals. The proposed amplifiers are designed to at least reproduce signals defined in [8].

$$V_r(t) = \sum_{n=0}^{N} A_n e^{-\alpha_n t} cos(\omega_n t + \phi_n), \quad (5)$$

where A_n are the amplitudes of N sinusoidal components, α_n the damping factors of their exponential envelopes, ω_n and ϕ_n are the frequency and phase of each component,

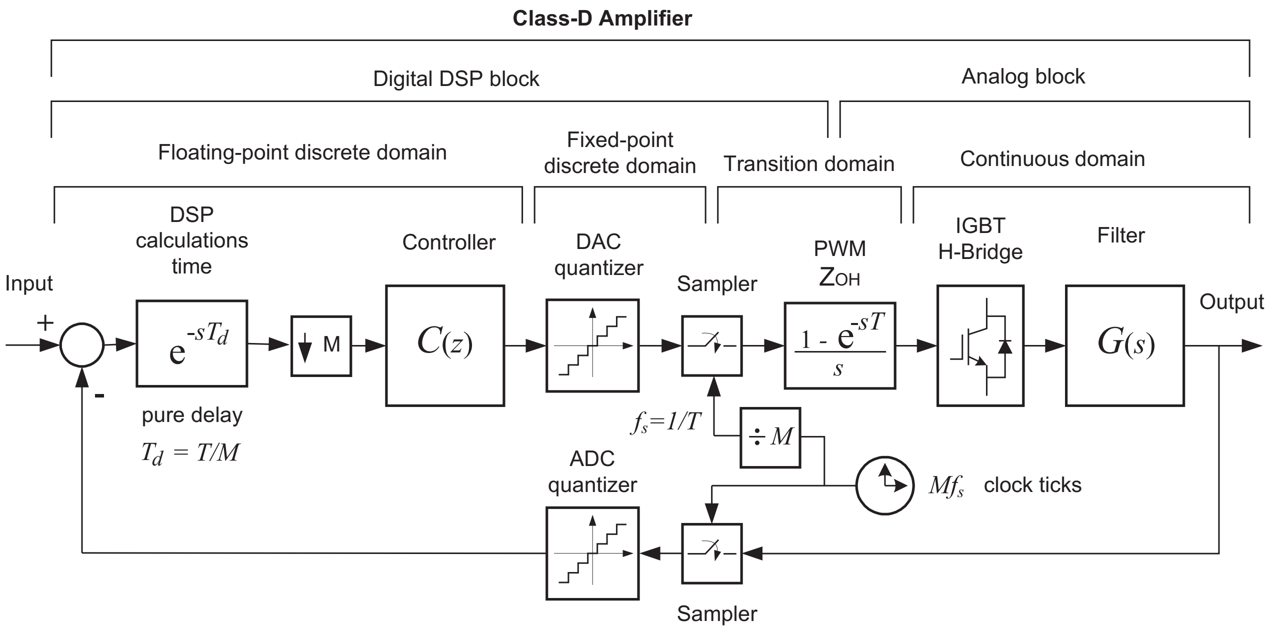

Fig. 3. Dynamic model for the proposed ampliflers.

respectively. For $\omega_n = 0$ we represent the DC decaying exponential, and there is no restriction on the frequencies ω_n which requires they to be integer multiples of any fundamental. Only a maximum frequency of 3kHz is established in the present work, concerned with relaying demands and the design investigation.

The amplifier block presented in the Fig. 3, and described previously with the new improved controller, has an internal feedback controller to follow the reference signal for different relay input impedances. Fig. 5 shows the closed-loop frequency response of this amplifier. One can note that both the magnitude and phase responses make the amplifier unable to achieve an accurate reproducibility up to 3kHz. In order to extend the operating band up to 3kHz, we adopt the use of a FIR compensator to correct the phase and magnitude of the desired signal. The parameters of class D amplifier, and the filter embedded in the controller are: $L = L_A = 500\mu H$, $C = C_A = 3.1\mu F$, $C_d = 1nF$, $R_A = 0$, $R_c = 1k\Omega$ and a PI controller with $k_p = 10$ and $k_i = 120$, $f = 60kHz$.

Compensation filter

Fig. 6 presents the block diagram of the proposed compensated voltage amplifier. A compensation FIR filter modifies the reference signal applied to the amplifier input in order to mitigate the previous mentioned magnitude and phase distortions. The filter coefficients are estimated using an LMS algorithm [12,13] for each signal to be played back, before the relay test. During the training period, a sequence of the reference signal is generated many times until the LMS algorithm convergence [12,13]. The open-loop transfer function for the amplifier block is written as

$$H(s) = \frac{1 - e^{-Ts}}{sT} C(s) G(s) V_{DC}, \tag{6}$$

where $C(s)$ is a PI controller, $G(s)$ is the inductor-capacitor low-pass LC filter, V_{DC} the power supply voltage, $e^{-T_d s}$ is related to the computational delay T_d , and $\frac{1-e^{-Ts}}{sT}$ the zero-order hold for a sampling period T. The LC filter is designed to eliminate harmonics produced by PWM switching. The frequency response of the class-D amplifier for unit gain closed-loop negative-feedback, given by $\frac{H(s)}{1+H(s)}$, is that presented in Fig. 5. The ZOH dynamic response is equivalent to a delay of $T/2$, which have some dominance on the phase and magnitude of the reconstructed output signal. The controller would have to be non-causal to compensate the ZOH dynamics. The consequences can be observed also in Fig. 5, i.e., it is impossible to obtain a flat gain without phase lag, even using quasi-optimal PI tuning. However, for low frequencies

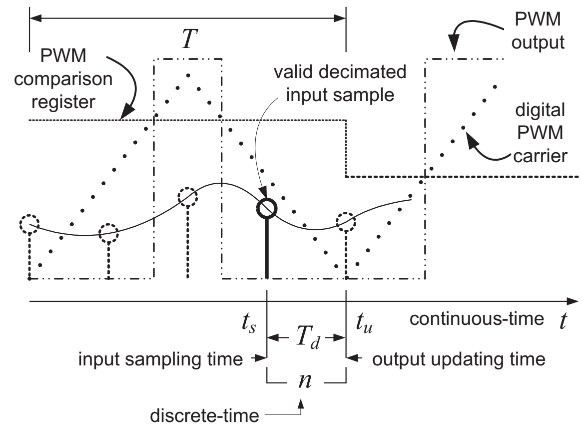

Fig. 4. System timing and delays.

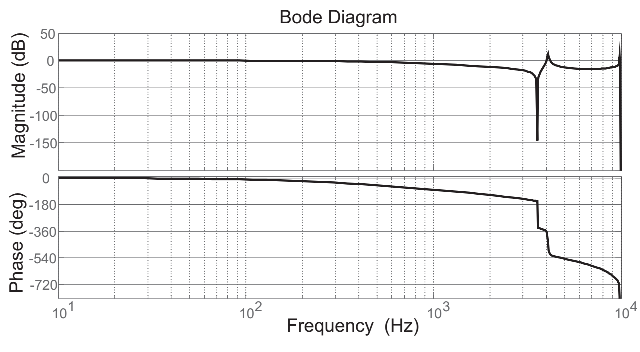

Fig. 5. Frequency response of the power voltage amplifier, effect of ZOH and delay.

at 50/60Hz the controller follows the reference signal with a minimum error, and the mentioned considerations are irrelevant in the design of inverters. The design of current amplifiers follows the same above mentioned approach and is not presented in this paper.

LMS Algorithm

The LMS algorithm [13] provides weight coefficients to the FIR filter, which are updated according to

$$w[n+1] = w[n] + \mu e[n]x[n], \tag{7}$$

where μ is the step size, $w[n]$ are calculated to minimize an error $e[n] = d[n] - y[n]$ between the desired reference signal $d[n]$ and the discrete form of the amplifier output signal $y[n]$. Fig. 6 presents the block diagram of the proposed compensated amplifier. The protective relay test is done in two steps: First, the LMS filter estimates the weights $w[n]$ using a delayed version $d[n] = x[n-N]$of the previous generated reference signal. This N samples delay is required to give the filter a causal margin to adjust itself. The reference signal $x[n]$ is repeated as many times as necessary to achieve the desired convergence error. When this occurs, the LMS algorithm immediately stops and the weight coefficients $w[n]$ are frozen and transferred to the FIR filter. Second, the relay can be tested since the FIR filter compensates the frequency response at the expense of introducing N sample delays in the output signal, and the real playback test is accomplished. This delay has no effect on the testing result.

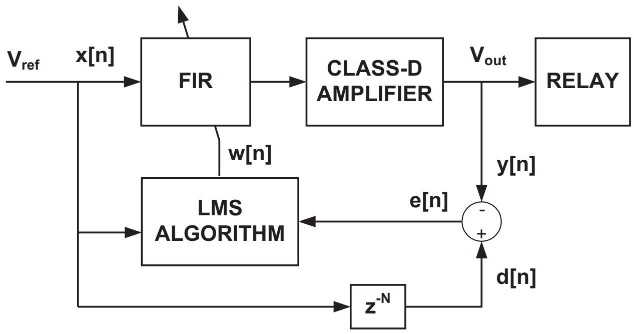

Fig. 6. The block diagram of the proposed technique.

Results

Test procedures include stead-state and transient signals obtained from a digital fault recorder or produced by a simulation program, such as EMTP or MATLAB. The signals may be recorded as COMTRADE or WAV files and can be played back using digital-to-analog converters or PC audio outputs. A 20kHz sampling frequency was employed to acquire the reference signal, which is the same switching frequency of the PWM-driven IBGT output bridge. The corresponding amplified signal was connected to the relay input. The proposed amplifier has been simulated for different types of signals in the bandwidth ranging from DC to 3kHz or to the 50^{th} harmonic. The FIR filter compensation made the amplifier capable of reproducing accurately the signals of different spectral features. To see the pronounced effects of the compensation, we chose a single frequency signal of 2.8kHz, where the magnitude and phase distortions are evident. The better results were obtained using: N = 16 sample delays; the FIR filter having 64 coefficients; and the LMS algorithm with an adaptation step size of 0.1. Fig. 7 presents the output and reference signals at 2.8kHz without the FIR filter compensation. It is observed that the amplifier cannot compensate the desired magnitude and phase response, with similar distortion values as depicted in Fig. 5. Fig. 8 shows the output and reference signals at 2.8kHz with the FIR filter compensation. It can be seen clearly that both magnitude and phase have their distortions mitigated and are in good agreement with the desired response. In Fig. 9 the response for a transient with harmonic components was generated following the same comparison as in [8]. Differently from the previous paper, Fig. 9 shows that the desired signal was produced at the output of the power amplifier without both attenuation and phase delay, showing the effect of the FIR adaptive compensator.

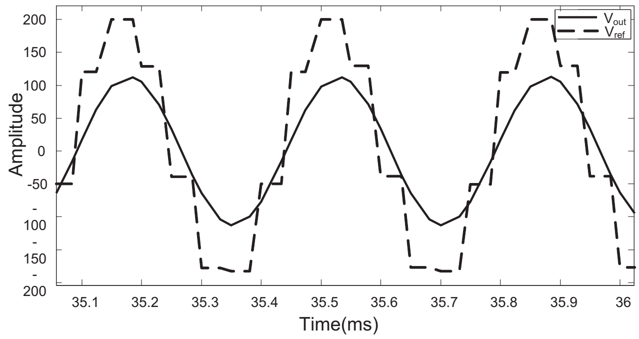

Fig. 7. Output and reference signals at 2.8kHz without the compensation.

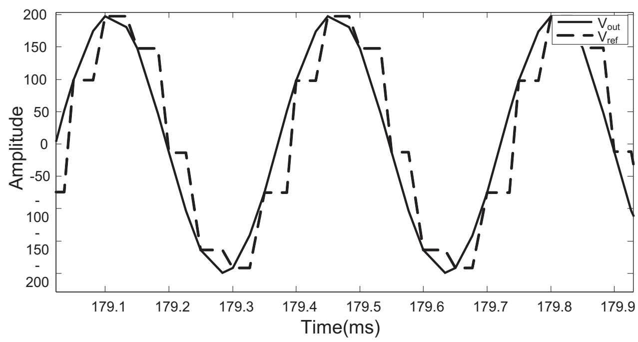

Fig. 8. Output and reference signals at 2.8kHz using compensation.

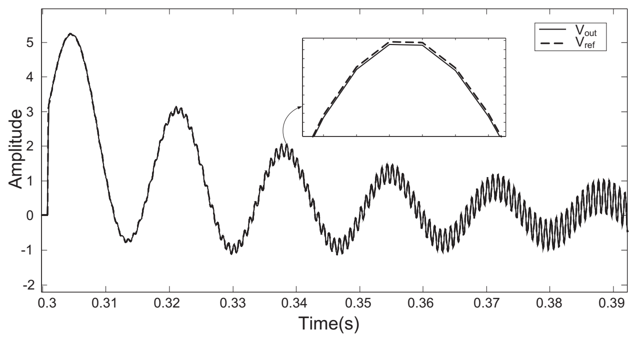

Fig. 9. Simulation of a transient current signal with exponentially decaying DC component and increasing harmonic of 1.2 kHz.

Conclusion

An LMS-based adaptive frequency compensator was proposed and presented to extend the bandwidth of a previous amplifier design from 1.2 to 3kHz. Simulation results have been presented for typical faults and multi-harmonic signals usually found in protective relay test. However, as the frequency increases, the original controller becomes gradually unable to compensate, especially at the upper end of the spectrum of 3kHz. To compensate the phase and magnitude, we presented a solution to the problem by inserting an LMS adaptive filter between the controller and the reference signal to correct the undesired distortions. The simulation results show that it is possible to mitigate the phase and magnitude distortion caused by the low switching frequency of IGBT transistors. Thus, it is possible to generate signals that can emulate the high ratings of current and voltage transformers for frequencies in the range of DC to 3kHz. The proposed frequency compensation technique has the potential to design voltage and current amplifiers suitable for field protective relay testing in utilities or research applications.

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