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Simulation Analysis of Geometrical Parameters of Monolithic On-Chip Transformers on Silicon Substrates

Abstract. *In this work, we study the effect of the geometrical parameters of on chip transformer, so to establish a methodology of its dimensioning and consequently its integration in a chip. The inductance and thus the quality factor of the monolithic transformer depend on the geometry of the transformer. Therefore, the geometry of the transformer needs to be optimized to give better quality factor (primary or secondary) and the inductance of the transformer (primary or secondary). The various geometric parameters that influence the performance of the transformer: Our aim is the monolithic or hybrid integration of this type of transformer in power device.*

Streszczenie. *W artykule analizowano wpływ geometrii scalonego transformatora na jego właściwości. Analizowano monolityczny transformator naniesikony na podłoże krzemowe.* ***Analiza parametrów geometrycznych monolitycznego transformatora na podłożu krzemowym***

Keywords: Monolithic On-chip transformer, Geometrical parameters, Electrical parameters.
Słowa kluczowe: tranmsformator monolityczny, geometria transformatora.

Introduction

If the power supply had only few interests of research in the past, it is today recognized like the major stake to surmount for the next portable electronics generations; power supplies are adapted to various applications via the static converters.

The integration of various elements composing a static converter, in particular the passive components, became the main aim today in the field of the power electronics.

The monolithic or hybrid integration of semiconductors generated real progress, but the passive components which lend themselves less easily to these techniques, slow down the complete integration of monolithic transformer. It is thus necessary to undertake research on the integration of the passive components.

In recent years monolithic transformers have been successfully implemented in RFIC designs. At the time of this writing, monolithic transformers fabricated on silicon substrates are used in silicon RF IC's enabling the implementation of high frequency circuits such as Low Noise Amplifiers (LNAs) [1, 2], Voltage-Controlled Oscillators (VCOs) [2, 3], and mixers [4, 5].

Transformers have been used in radio frequency circuits since the early days of telegraphy. The transformers are important elements in many different applications such as power combining, signal coupling, bandwidth enhancement, and common-mode rejection.

Planar integrated transformer can have different geometries. They can be square, rectangular, circular, etc. it is worth checking whether the geometry makes a difference in terms of Q factor. In this paper we have characterized both square transformers.

The inductance and thus the quality factor of the transformer depend on the geometry of the transformer. Therefore, the geometry of the transformer needs to be optimized to give better quality factor and inductance. The various geometric parameters that influence the performance of the transformer as listed below and shown is figure 1:

- Outer diameter of the transformer OD.
- Number of turns N.
- Width of metal traces W.
- Spacing between turns S.

The transformer will be modelled and simulated to further verify whether process parameters are well calibrated or not.

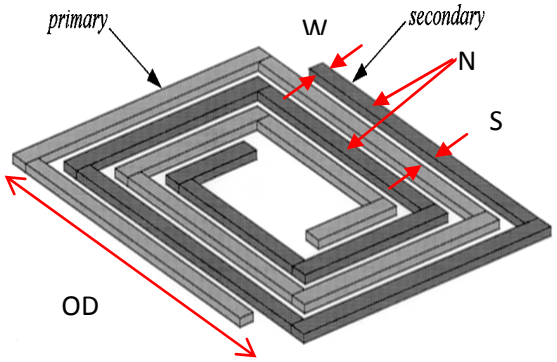

Fig. 1. Various geometrical parameter of the transformer.

The transformer has the same metal width and metal spacing as well as the different number of turn and the outer diameter. Therefore, effects of the number of turn, conductor width, winding separation or spacing and the outer diameter on the transformer performance will be discussed.

Monolithic Transformer Topologies

In the monolithic implementation of transformers, the metal windings can be laid out physically on the silicon substrate in different ways. Depending on the layout, these transformers can be broadly classified into two types, namely, stacked transformer and interleaved transformer [6]. Several variants of these transformers were developed and experimented in the past [7]. All these structures have both advantages and disadvantages, and so the transformer that best suits the application can be chosen.

Stacked Transformer

The primary and secondary metal windings of the stacked transformers are laid on top of each other on the silicon substrate, i.e., the two windings are stacked one above the other [8, 9]. As a result, the area occupied is less when compared to that of interleaved transformers. Here, the vertical coupling of the magnetic field between the primary and secondary winding dominates over the edge coupling between the windings [10]. The top view and side view of a stacked transformer is shown in figure 2. Since the spacing between the metal layers is less when compared to the spacing between the metals in the same plane, the mutual inductance between the windings is comparatively high in stacked transformers.

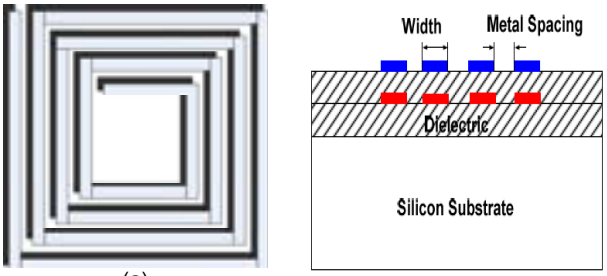

Fig. 2. (a) Top view of four-port stacked transformer on silicon substrate, (b) Side view of stacked transformer on silicon substrate.

However, since the two windings are on top of each other and closely spaced, the electric coupling between the windings is more when compared to that of the interleaved transformers, and so the interwinding capacitances are higher compared to those of interleaved transformers. Stacked transformers are not symmetric because one winding is closer to the substrate. The top winding is shielded from the substrate by the bottom winding, and so the substrate losses are less in the top winding compared to the bottom winding. Another reason for the asymmetric nature of stacked transformers is that the metals in different layers typically have different thicknesses.

Interleaved Transformer

For the interleaved transformers, the primary and secondary metal windings are interwound in one plane [11, 12] as shown in figure 3. Hence, the area occupied is larger compared to the stacked transformers [13]. Here, the nesting of the windings with larger spacing results in reduced flux linkage between the primary and secondary windings compared to stacked configurations. Hence, the mutual inductance is reduced in interleaved transformers. Also, the electric coupling, which is the result of edge coupling between the two windings, is reduced compared to stacked transformers, and so the interwinding capacitances are less compared to stacked transformers. Interleaved transformers are symmetric because the windings are in the same plane and laid out symmetrically.

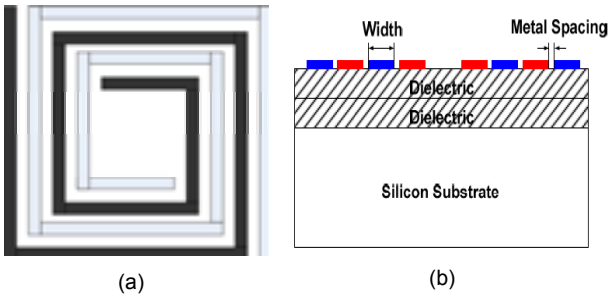

Fig. 3. (a) Top view of four-port interleaved transformer on silicon substrate. (b) Side view of interleaved transformer on silicon substrate.

Equivalent Circuit Model for Transformer

Figure 4 (a) and (b) show its compact equivalent circuit model of a silicon transformer and simplified model for transformer, respectively. As shown in Figure 4(b), the primary and secondary coils of the transformer can be equivalent to have series resistances (Rp, Rs) and series inductances (Lp, Ls), with a mutual inductance denoted by M [14].

In figure 4 (a) shows an equivalent circuit model for the on chip transformer, which consists of more than twenty (20) parameters, the following are considered [15, 16]:

- Ls,p and Ls,s represent the series inductance of the primary and the secondary coil, respectively. The magnetic flux between coils is modelled by coupling coefficient K, is calculated by following equation:

$$k = \frac{M}{\sqrt{L_p . L_s}} \quad (1)$$

- The ohmic loss dissipated in the conductors is represented by the series resistances Rs,p and Rs,s of the primary and the secondary coil, respectively.
- Cp,ps and Cp,sp model the parasitic capacitive coupling between primary and secondary coils.
- Cp,pp and Cp,ss model the parasitic capacitance between metal wires of the primary and the secondary coil, respectively.
- (Cox.1 to Cox.4) and (Cox.3, Cox.4) are the oxide capacitances between the turns of the primary coil and the oxide and the turns of secondary coil and the oxide, respectively.
- (Csi,1 to Csi,4) model the parasitic capacitance of the silicon substrate.
- (Rsi,1 to Rsi,4) represent the resistance loss of the silicon substrate.

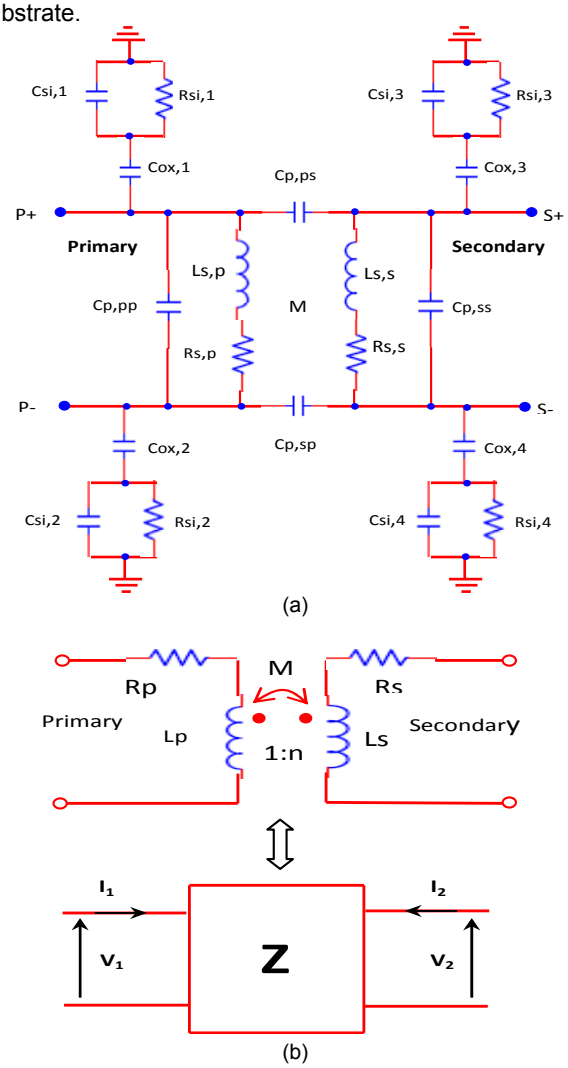

Fig. 4. (a) Compact equivalent circuit model of a silicon transformer, (b) Simplified model for transformer.

To analyze the overall model performance, a transformer configuration of the circuit shown in figure (4.a) with ports and 4 grounded was used. The resulting two-port impedance matrix was analyzed using the following

commonly used quantities to evaluate model performance. The Z parameters model can be represented as a simplified lumped transformer model (figure 4(b)). According to current and voltage expressions, the impedance matrix is given by:

$$(2) \qquad [Z]=\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix}=\begin{bmatrix} R_p+j\omega L_p & j\omega M \\ j\omega M & R_s+j\omega L_s \end{bmatrix}$$

In the formulas shown below $\omega = 2\pi f$, where f is the frequency of operation in Hertz (Hz).

The self inductances (Lp, Ls) and resistance (Rp, Rs) of the primary and the secondary coils respectively. They are extracted using the following equations [17, 18]:

$$(3) \qquad L_p = \frac{\mathrm{Im}(Z_{11})}{2.\pi.f}$$

$$(4) \qquad L_s = \frac{\mathrm{Im}(Z_{22})}{2.\pi.f}$$

$$(5) \qquad R_p = \mathrm{Re}(Z_{11})$$

$$(6) \qquad R_s = \mathrm{Re}(Z_{22})$$

Qp and Qs are the quality factors of the primary and secondary coils. They are given in terms of the Z-parameters as:

$$(7) \qquad Q_p = \frac{\mathrm{Im}(Z_{11})}{\mathrm{Re}(Z_{11})}$$

$$(8) \qquad Q_s = \frac{\mathrm{Im}(Z_{22})}{\mathrm{Re}(Z_{22})}$$

Results and Discussion

A monolithic transformer was simulated with MATLAB, to validate the electrical model. The key geometrical parameters are outer diameter *OD*, number of primary turns *Np*, number of secondary turns *Ns*, width of metal traces *W*, spacing between the traces *S*. the thickness of the top metal layer *t* and the length of primary turns *lp*.

Influence of the outer diameter OD

Increasing the outer diameter *OD* results in an increase of the conductor length and the area occupied by the transformer, the inductance *Lp* for three values of outer diameter *OD* (100µm, 200µm and 300µm) are shown in figure (5). The primary inductances are calculated according to equation (3). The transformer with longer conductor length has larger *Lp* according to the electromagnetic principle. It also can be observed that the self resonant frequency decreases with increasing the outer diameter *OD* for transformers. The self resonant frequency is dominated by the capacitance to the substrate (C_{ox} and C_{sub}). The capacitance to the substrate increases with the increasing area.

Figure (6) shows the effect of the outer diameter *OD* on quality factor *Qp*. The primary quality factors are calculated according to equation (7). Quality factor *Qp* decreases with the increase of the outer diameter. The transformer with larger area has lower *Qp*, which is because the larger area suffers from larger substrate loss.

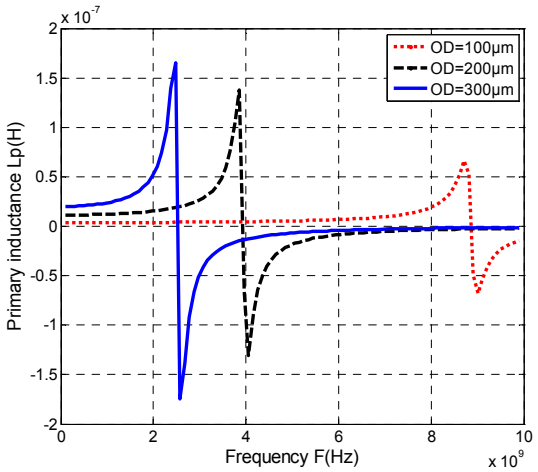

Fig.5. Primary inductance Lp as a function of frequency and outer diameter OD (100µm, 200µm and 300µm).

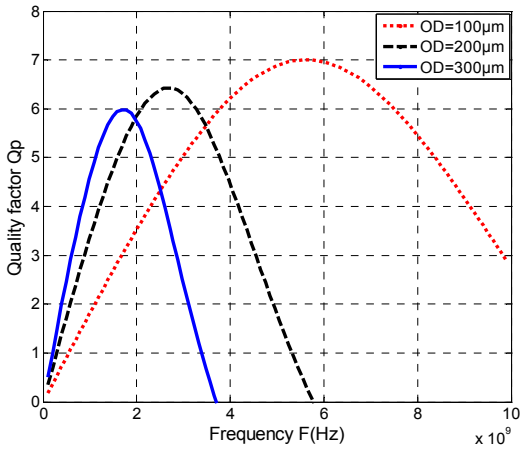

Fig. 6. Primary quality factor Qp as a function of frequency and outer diameter OD (100µm, 200µm and 300µm).

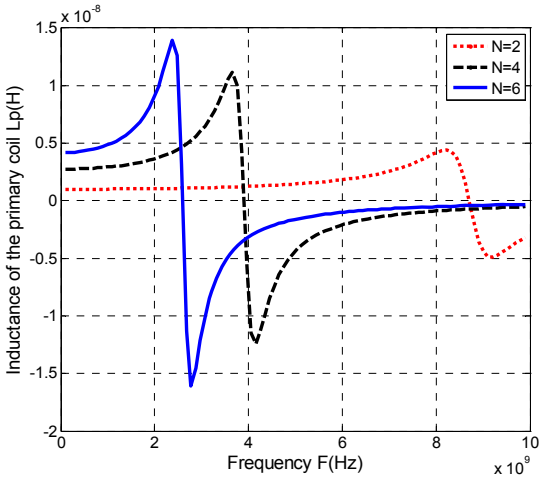

Fig.7. Primary inductance Lp as a function of frequency and number of turns N (2, 4 and 6).

Influence of the number of turns N

The second obvious parameter is the number of turns *N* of the transformer. The inductance *Lp* and quality factor *Qp* for three values of N (2, 4 and 6) are shown in figures (7,8). The inductance *Lp* value increases when the transformer has more turns. However, from figure (7), we can deduce that the inductance *Lp* value does not increase linearly with the number of turns, as the area of the inner windings (loop area) is smaller compared to the outer windings since the outer size of the transformer is kept constant. The self-

resonance frequency (where the inductance *Lp* value goes through a zero and capacitive effects start to dominate the behaviour of the transformer) decreases significantly for each new turn added because of the increased capacitive coupling between the turns and the increased capacitive coupling to the substrate. The maximum quality factor *Qp* also decreases significantly with increasing *N* because the increased metal loss, as shown in figure (8). The quality factor peak is 6.3, 6.9 and 7.5 at 2.9, 3.9 and 5.5 GHz, respectively, for transformers with six, four and two turns.

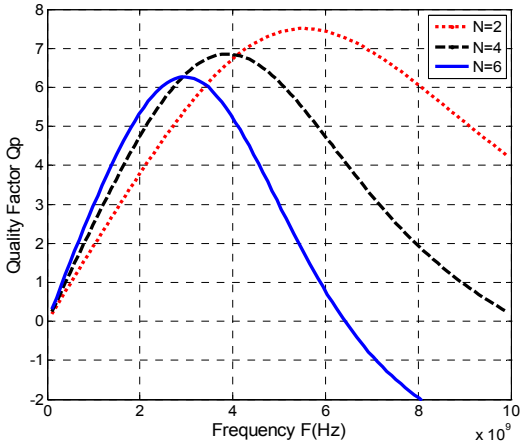

Fig.8. Primary quality factor Qp as a function of frequency and number of turns N (2, 4 and 6).

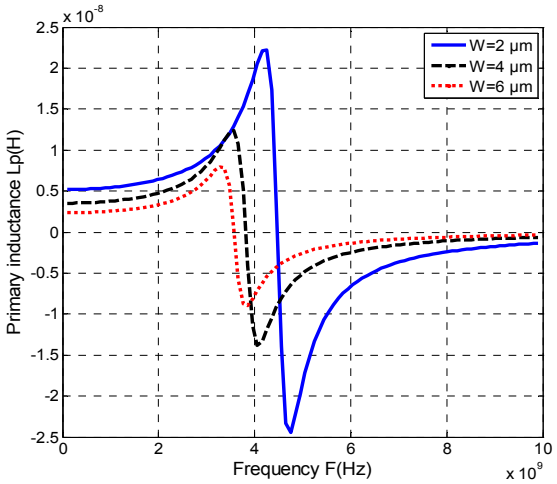

Fig.9. Primary inductance Lp as a function of frequency and width of metal traces W (2μm, 4μm and 6μm).

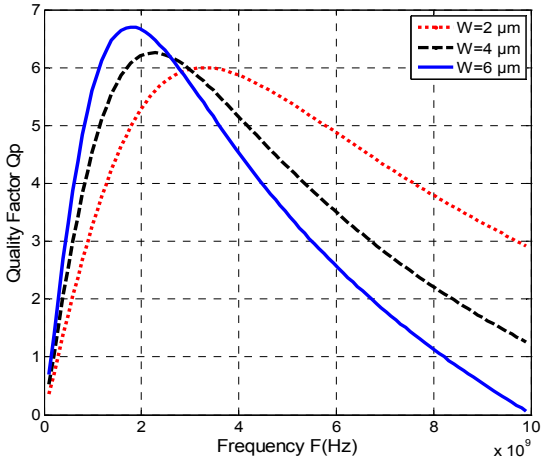

Fig. 10. Primary quality factor Qp as a function of frequency and width of metal traces W (2μm, 4μm and 6μm).

Influence of the width of metal traces W

The width of the metal trace affects the performance of the inductor to very large extent, as shown in figures (9,10).In figure (9), the width of the metal traces *W* is varied from (2μm to 6μm). The inductance *Lp* value decreases as the loop area of the inner windings decreases with increasing width, but the self resonance decreases because of the larger capacitive coupling of the metal traces to the substrate. The quality factor *Qp* decreases with increasing metal width because of the skin effect in the metal layer that leads to current crowding to the edges of the conductor. The lower self-resonant frequency due to larger metal width occurs because of larger capacitive coupling of the metal traces to the substrate. Therefore, the metal width should be as wide as possible so as to achieve a low resistance. Larger width implies larger area transformer and hence larger parasitic capacitance, skin effect, and substrate loss. The width of the coil conductor should only be large enough to reduce the ohmic loss in the transformer structure, only increases the maximum quality factor from (4.2 to 5.7), as shown in figure (10).

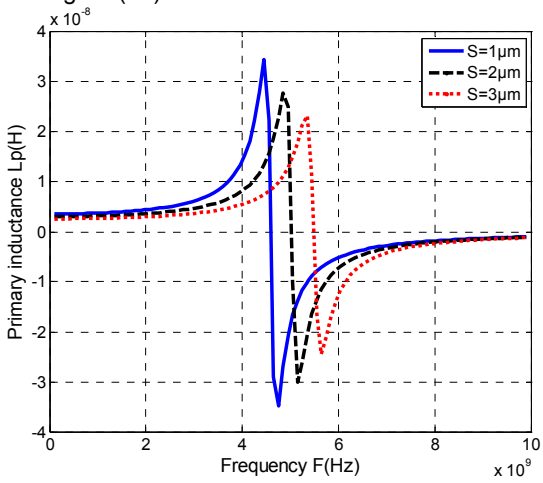

Fig. 11. Primary inductance Lp as a function of frequency and spacing between the traces S (1μm, 2μm and 3μm).

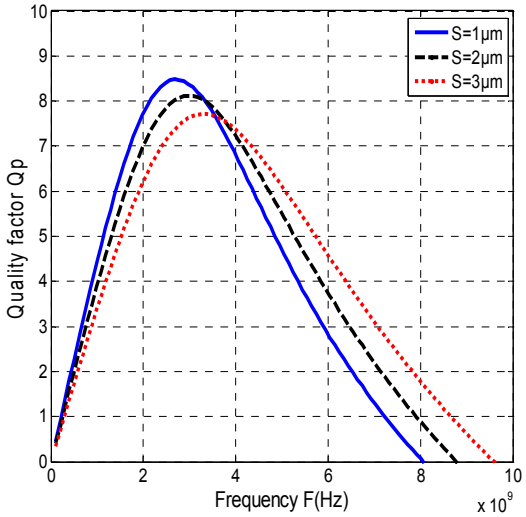

Fig. 12. Primary quality factor Qp as a function of frequency and spacing between the traces S (1μm, 2μm and 3μm).

Influence of the spacing between the traces S

In figure (11), the effects of varying the separation distance between the turns, *S*, from (1μm to 3μm). The inductance *Lp* value decreases with increasing *S*. Increased spacing between the metal traces leads to lower inductance due to decreased magnetic coupling between the segments and increased metal resistance. Smaller separation

distances result in higher capacitive coupling between the turns and therefore a lower self resonance frequency. The maximum of the quality factor *Qp* is not so sensitive to the separation distance, shown in figure (12).

Conclusion

In this work we presented a compact integrated silicon technology transformer electric model. The model is extracted taking into account the physical aspects of the transformer both layout and in terms of technology level. This model is as simple as precise to be used effectively in the design of RF circuits. Then we varied the geometrical parameters (the outer diameter OD, number of turns N, conductor width W, the space between two coils S to see their influence on the electrical response of the transformer.

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