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Dual mode 4th order active-RC low-pass filter with tunable cut-off frequency from 3 MHz to 20 MHz in 65 nm CMOS

Abstract. In this paper, a 4th order active-RC filter with two approximation modes and a tunable bandwidth from 3 MHz to 20 MHz is presented. The filter can be configured to achieve maximally flat in-band magnitude or phase response by using a dual mode resistor bank and has gain control. PVT induced parameter drift compensation is accomplished by using a reduced-in-size resistor bank structure made of series and parallel connected resistors. Furthermore, a design method for the resistor bank is presented, that allows component value calculation based on accuracy and tuning step requirements. The power dissipation is bandwidth depended and ranges from 13 mW to 23 mW from a 1.2 V supply for the entire tuning range, while the SFDR is higher than 72 dB and 65 dB at min and max bandwidth settings respectively. The proposed filter is designed and its parameters verified by using 65 nm CMOS technology and occupy a layout area of 0.172mm².

Streszczenie. W artykule przedstawiony aktywny RC filtr dolnoprzepustowy czwartego rzędu z dwoma trybami aproksymacji i przestrajaną częstotliwością graniczną od 3 MHz do 20 MHz w technologii 65 nm CMOS. Przedstawiono też metodę projektowania zestawu rezystorów, która umożliwia obliczenie wartości składnika w oparciu na wymagania dokładności i kroku regulowania. (Aktywny RC filtr dolnoprzepustowy czwartego rzędu z przestrajaną częstotliwością graniczną od 3 MHz do 20 MHz w technologii 65 nm CMOS).

Keywords: active-RC, approximation, resistor bank, tuning, value calculation, variable.

Słowa kluczowe: aktywny filtr RC, aproksymacja, zestaw rezystorów, przestrajanie, zmienna.

Introduction

One of the properties of modern wireless base station is the ability to work on several different wireless standards [1, 2]. In order to send or receive multi-standard signals, wireless hardware is needed, whose parameters could be changed depending on requirements, which are defined by wireless standard. Wireless device, which can operate on a variety of different mobile standards, is called multi-standard transceiver [3, 4]. The function of data channel selection is performed by analog and digital filters [5, 6]. Analog filters with configurable bandwidth and approximation functions have been gaining attention, since they form either the front-end or the back-end for the analog-to-digital or vice versa converters [7, 8].

A variety of different types of continuous-time filters can be used in modern transceivers, including, but not limited to, gm-C, current-mode and active-RC filters. Although discrete-time switched-capacitor filters can also be used in transceivers, the need for additional aliasing filters, high frequency clock distribution networks, larger unity-gain-bandwidth of operational amplifier (OA) requirements and noise levels limit their use as wideband channel selection filters.

Active-RC low-pass filters, compared to filters mentioned above, exhibit the highest output dynamic range and low noise level [9]. However, the main disadvantage of such filters is their sensitivity of bandwidth and gain to variations of values of filter-composing elements. Variations of elements in integrated circuits (IC) originate due to temperature variation, ageing or inconsistency of IC manufacturing process (PVT). Variations of parameters of analog blocks in multi standard transceiver induce amplitude and/or phase offsets of quadrature signals in respect of each other. Therefore, it increases distortion of signals, which are being sent or received [10]. Variation of filter parameters due to PVT is compensated by using digitally controllable resistor and/or capacitor banks [11, 12]. For a filter with reconfigurable pass-band, capacitor banks are usually used to select the desired bandwidth, while resistor banks are used for PVT calibration routines. In this case, accuracy and tuning range of calibration depend on structure of resistor bank and number of values of control signal. To achieve small tuning step over a wide tuning

range (which can be as high as 40% of filter's bandwidth), resistor banks that occupy large area of silicon are needed.

In this work, a structure of resistor bank is proposed, that minimizes the total value of resistance of the resistor bank, which is needed to achieve accurate filter's bandwidth and gain tuning. Furthermore, a design procedure is presented that is used to calculate the values of resistor bank components based on the required tuning range and accuracy. The reduction of layout area is exploited by using a structure of dual-mode resistor, which enables the filter to have either maximally flat in-band amplitude or phase responses (Bessel or Legendre approximations). The structure of dual mode resistor bank is used in a 4th order ladder filter design with configurable bandwidth from 3MHz to 20MHz, which complies with common channel bandwidths of LTE standard.

This paper is organized as follows: first, the structure of the proposed resistor bank and its design procedure is analysed. In the next section, structure of designed filter, including its OA, is presented, followed by discussion of simulation results and conclusions.

Structure of dual mode resistor bank

Resistor banks in active-RC filters with discrete-step tuning control are usually designed by connecting n number of MOS-switched resistors in parallel with resistor of fixed value. This type of structure is called parallel connected resistor bank (PRB) and is shown in Fig. 1 a). By setting resistor values to $R_{Ln}/2^n$, a resistor bank with wide tuning range can be implemented by using only several resistors [13]. One major disadvantage of PRM structure is the need for high value resistors if wide tuning range with a small maximum step size is needed. The network of resistor ladder, formed from a string of resistors or by using R-2R ladder, can be used to design resistor banks with small tuning step, but they require a high number of MOS switches and resistors and are usually used with a limited amount of control settings [14]. Furthermore, in the case of R-2R ladder, the current steering nature of this structure degrades the noise performance of the active-RC filter.

The proposed resistor bank is shown in Fig. 1 b). The structure is composed of parallel and series connected resistor banks (SPRB), which are controlled by a separate control lines. Series connected resistor bank (SRB) is used

to select the coarse resistor value, and PRB is used to achieve fine tuning of the desired resistance. The SRB is controlled by a binary-coded decimal control while the PRB is controlled by binary control code. As stated, if only PRB is used, high value resistors are needed to achieve a small control step size ($< 1\%$ of filter's bandwidth). By using the proposed combination of both tuning banks, the resistor values in the PRB can be reduced by a factor of k while maintaining the required tuning accuracy.

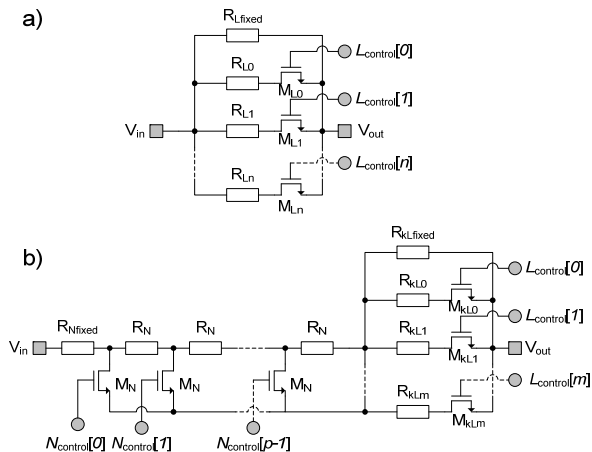


Figure 1. a) – parallel connected resistor tuning bank (PRB); b) – proposed series and parallel connected resistor tuning bank (SPRB)

The value of SPRB resistor $R_{kLfixed}$, as shown in (1), depends on the wanted total resistance value of resistor bank and the tuning range, needed for particular IC process induced variations. In this case, the minimum needed resistance value can be expressed as shown in (2).

$$(1) \quad R_{kLfixed} = \frac{R}{k} \cdot \left(1 + \frac{\Delta\omega}{100\%} \right)$$

$$(2) \quad R_{kLmin} = \frac{R}{k} \cdot \left(1 - \frac{\Delta\omega}{100\%} \right)$$

where: $\Delta\omega$ – wanted tuning range of filter's bandwidth, expressed in percentage.

Resistor's value, needed to change the tuning bank with a maximum step size of φ_{step} is calculated from (3).

$$(3) \quad R_{kL} = \frac{100\% \cdot R_{kLfixed}^2}{R \cdot \varphi_{step}} - R_{kLfixed}$$

where: φ_{step} – the maximum tuning step from the desired frequency in the whole resistor bank tuning range expressed as percentage.

Next, the minimum PRB control code value m , which meets the maximum step size φ_{step} requirement, is calculated according to (4)-(6).

$$(4) \quad m = \begin{cases} \alpha, & \beta > 1 \\ \alpha + 1, & \beta \leq 1 \end{cases}$$

$$(5) \quad \alpha = \left\lceil \log_2 \left(\frac{2 \cdot R_{kLfixed} \cdot \Delta\omega}{R \cdot \varphi_{step}} \right) \right\rceil$$

$$(6) \quad \beta = \frac{R_{kLmin} \left(R_{kLfixed} + \left(\frac{R_{kL}}{2^\alpha} \right) \right)}{R_{kLfixed} \cdot \left(\frac{R_{kL}}{2^\alpha} \right)}$$

Values of PRB resistor R_{kL0} and the remaining resistor R_{kLm} are calculated from (7). It can be seen, that the resistor values need to be reduced by a factor of 2 for each added

control bit. It is common, that the resistors in IC circuits are designed in equal segments which in turn are added in series or in parallel to achieve the required total resistance. This kind of approach is particularly useful for designing filter banks, whose resistors are increasing or decreasing by a factor of 2.

$$(7) \quad R_{kLm} = \frac{R_{kL}}{2^m}$$

SRB fixed resistor's value is then calculated from (8). The remaining values of resistors R_N are equal and can be found by using (9). The number of control MOSFETs M_N needed for the SRB is always equal to $R_{Nnumber}-1$, where $R_{Nnumber}$ is expressed by (10). It was mentioned, that the SRB control is implemented by using a binary-coded decimal code. The number of bits required to implement SRB control will differ from the number of M_N , and can be calculated from (11). The additional one control bit is added to fully switch off all MOSFET switches.

$$(8) \quad R_{Nfixed} = R_{kLmin} \cdot (k - 1)$$

$$(9) \quad R_N = R_{kLfixed} - R_{kLmin}$$

$$(10) \quad R_{Nnumber} = \frac{k \cdot (R_{kLfixed} - R_{kLmin})}{R_N} - 1$$

$$(11) \quad p = \lceil \log_2 (R_{Nnumber} + 1) \rceil$$

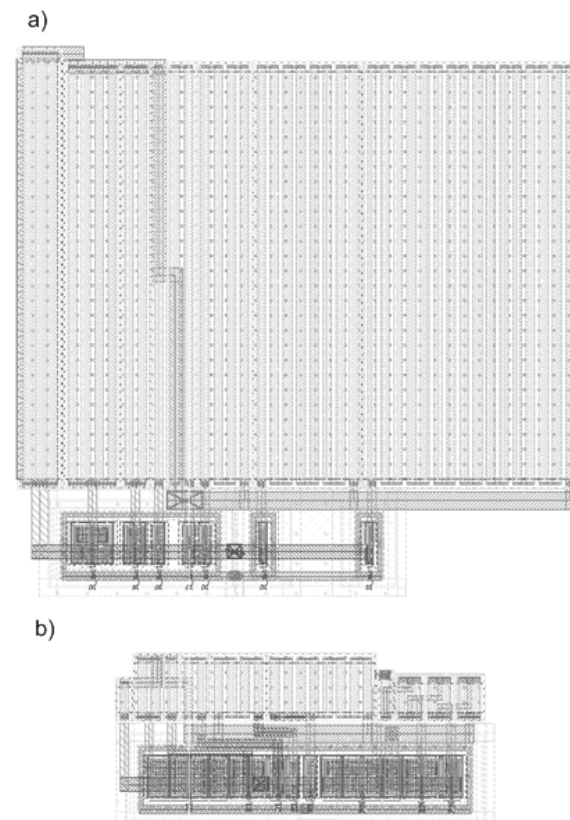


Figure 2. a) – PRB layout of 6 kΩ nominal value. Occupied area by resistors is 773 μm^2 ; b) – SPRB layout of 6 kΩ nominal value. Occupied area by resistors is 81.3 μm^2

The layout view of a PRB and SPRB structure with the same tuning range (40 %) and maximum step (1.5 %) is respectively shown in Fig. 2 a) and Fig. 2 b). Nominal value of resistance for both structures is set to 6 kΩ and the value of coefficient k for SPRB structure is equal to 4. Area occupied by resistors in PRB and SPRB structures are respectively equal to 773 μm^2 and 81.3 μm^2 . Resistor banks were designed using the equal segment approach described earlier, while their minimum width was kept

constant. It can be seen, that the proposed SPRB structure reduces the overall layout area, occupied by resistors, by more than 8 times when comparing it to the PRB structure.

With reduced-in-size resistor bank structure, active-RC filters with different approximations can be designed without sacrificing a lot of layout space. The structure of dual mode resistor used in the designed 4th order filter is shown in Fig. 3. The structure is made of two separate SPRB structures, designed to implement either Bessel (R_{BES}) or Legendre (R_{LEG}) approximations and controlled by EN_BES control signal. Full CMOS switches, made of PMOS and NMOS FETs, are used to isolate the unused resistor bank, while logic "AND" gates disable the $L_{control}$ and $N_{control}$ values for the same resistor bank. The use of full CMOS gates also reduces the switch related linearity distortion when the input signal level is close to the supply value.

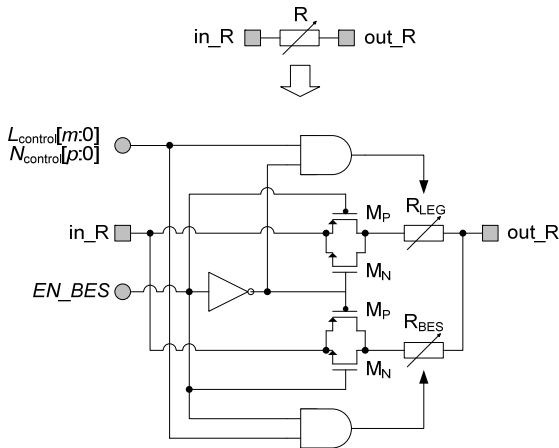


Figure 3. Implementation of dual mode resistor bank for active-RC filter approximation control

Filter design

The schematic of a fully differential dual mode 4th order active-RC low-pass filter with tunable cut-off frequency is shown in Fig. 4. The active filter uses a LC ladder structure due to its low sensitivity to component variation when comparing it to other filter structures [14]. The designed filter uses equal switched capacitor banks C , which share the same structure as PRB and are controlled by an 8 bit control signal. Differently sized (valued) resistor banks R_1 - R_6 are used to implement Bessel and Legendre approximations using the structures of dual mode resistor bank. SPRB were designed to achieve $\Delta\omega = 40\%$ and

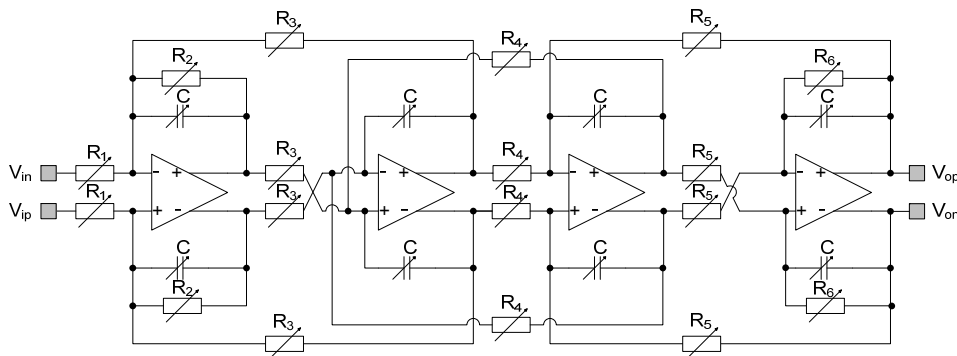


Figure 4. Schematic of the 4th order ladder filter

$\varphi_{step} = 1.5\%$. The number of control bits needed for $L_{control}$ and $N_{control}$ are calculated from equations (1)-(11) and are respectively equal to 5 and 2. An independent resistor bank control is used for R_1 to implement gain tuning, which is needed for active-RC filters used in quadrature paths of transceiver.

The schematic of fully differential OA used for all active blocks of 4th order ladder filter is shown in Fig. 5. Transistors M_3 and M_4 are used as inputs for the differential pair stage, while M_1 and M_2 are set as active loads biased by V_{ibias} (bias circuit not shown). M_5 transistor is used as the tail current source, whose bias current is set by the input stage of common mode amplifier circuit. The common mode amplifier, not shown here, is made of a differential pair similar to the input stage shown in Fig. 5 and is used to control the bias point of output stage and optimize the linear dynamic range of the filter by changing the V_{cmi} value. Similarly, the common mode voltage of output stage is controlled by a separate amplifier, which controls the V_{cmo} value of transistors M_9 and M_{10} . The output common mode voltage is fixed to half of the supply voltage. A controllable RC compensation network is used between the outputs of both input (V_{o1p} , V_{o1n}) and output (V_{op} , V_{on}) stages, where the control value is tied to the control value of filter capacitor bank.

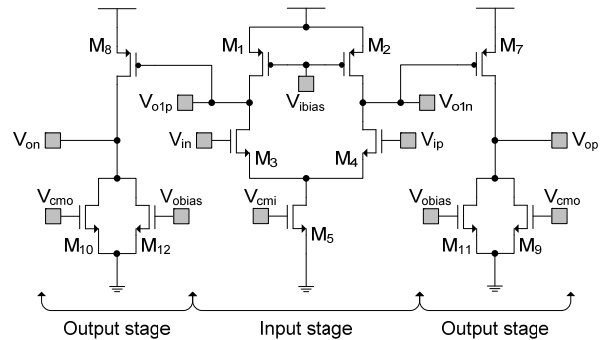


Figure 5. Schematic of the operational amplifier used in 4th order ladder filter

The layout of designed 4th order low pass filter, implemented in 65 nm CMOS IC process, is shown in Fig. 6. It occupies 0.172 mm² area of silicon.

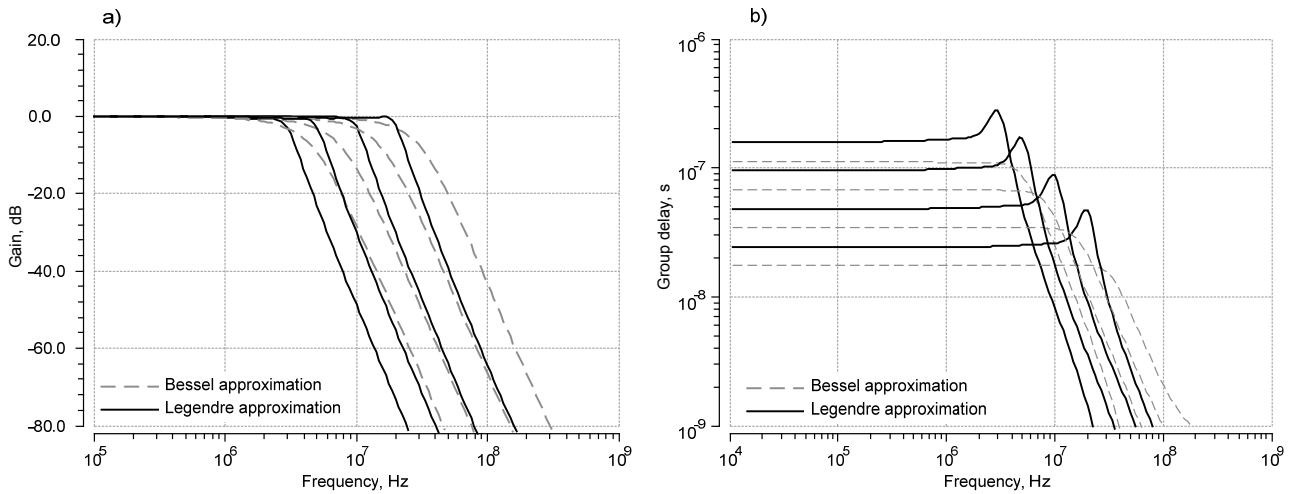


Figure 7. a) – magnitude response of the designed filter at both approximation settings; b) – group delay of the designed filter at both approximation settings

Simulation results

Supply voltage for the designed active-RC low-pass filter is 1.2 V. All results, provided in this section, are acquired from post-layout simulations.

The magnitude and group delay response for both approximation modes of designed filter are shown respectively in Fig. 7 a) and b), when the filter is configured for 3 MHz, 5 MHz, 10 MHz and 20 MHz bandwidth. It can be seen, that the filter can be tuned to exhibit both maximally flat in-band amplitude and maximally flat in-band phase response across its entire bandwidth tuning range.

The tuning range of the bandwidth of designed active-RC filter, using the SPRB structure at maximum bandwidth setting (20 MHz), when the filter is configured for Bessel approximation, is shown in Fig. 8. The simulation results show that the tuning range $\Delta\omega$ is equal to 39 %, which matches well with the initial design specification of 40 %. The maximum control step φ_{step} over the entire tune range is equal to 2 %. A difference of 0.5 % from the initial specification is present due to the unaccounted channel resistance of control MOSFET M_N and $M_{kl[4:0]}$ (see Fig. 1 b)) when the transistors are fully open. Increasing the size of the control transistor would reduce the error of tune step at the expense of increased layout area and additional parasitic capacitance. The obtained results hold for both Legendre approximation setting and for other bandwidth configurations.

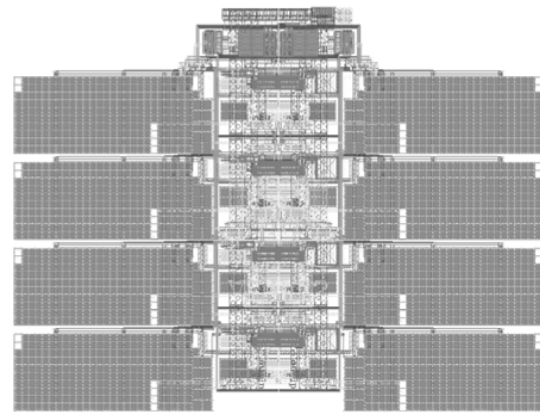


Figure 6. Layout of the 4th order ladder low pass filter

Tuning range of filter's gain is shown in Fig. 9. The simulation results were obtained with centred control values of SPRB resistors R_2 - R_6 . It can be seen, that the bandwidth of the filter is independent of R_1 gain control. The total gain control range is 7 dB, with a maximum gain step of 0.2 dB when Ncontrol is set to 0. However, absolute minimum and maximum gain levels would depend on the active control values of SPRB resistors R_2 - R_6 . Again, the obtained results hold for both Legendre approximation setting and for other bandwidth configurations.

Table 1. Main parameters of designed filter

Parameter	Filter configuration			
	Bandwidth = 3 MHz Bessel approx.	Bandwidth = 3 MHz Legendre approx..	Bandwidth = 20 MHz Bessel approx..	Bandwidth = 20 MHz Legendre approx..
Bandwidth tuning range [%]	39			
Bandwidth tuning step [%]	2			
Gain tuning range, dB	7			
Gain tuning maximum step [dB]	0.2			
In-band IIP3 (2,-1) (f1=0.5MHz; f2=0.7MHz) [dBm]	33.7	29.6	-	
In-band IIP3 (2,-1) (f1=3.9MHz; f2=4.1MHz) [dBm]	-		30.8	27.4
Integrated input-referred noise over the bandwidth [μ V]	60	50	130	119
Spurious-free dynamic range [dB]	74.1	72.3	67.1	65.5
Supply voltage [V]	1.2			
Power [mW]	12.9		22.9	
Area [mm ²]	0.172			

Main parameters of the filter are summarized in Table 1. For the linearity analysis of designed active-RC filter, two tone in-band IIP3 simulation with a 1 V_{pkpk} differential signal was performed at minimum (3 MHz) and maximum (20 MHz) bandwidth settings for both approximation modes. Frequencies of both test tones were set to 20 % of the bandwidth and separated by 200 kHz. The power dissipation of the filter is bandwidth dependent and is tuned by the controls of OA bias current. The designed filter dissipates 13 mW at 3 MHz and 23 mW at 20 MHz bandwidth settings. The spurious-free dynamic range is higher than 72 dB and 65 dB respectively for minimum and maximum bandwidth settings at both approximation modes.

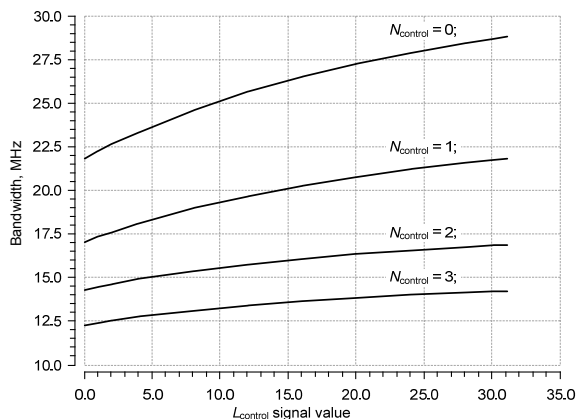


Figure 8. Bandwidth tuning range using SPRB controls

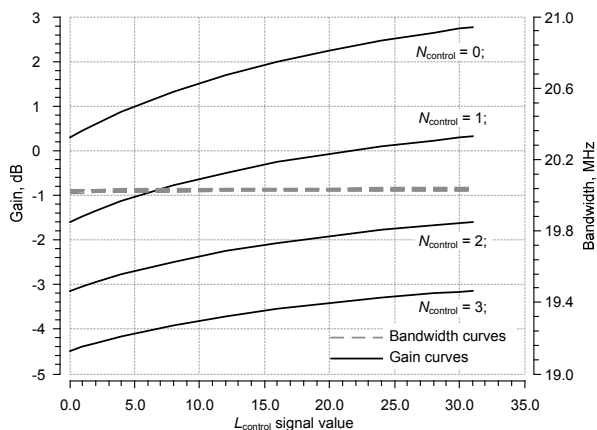


Figure 9. Gain tuning range using SPRB control for resistor R_1

Conclusions

A 4th order active-RC filter with two controllable approximation settings, Bessel or Legendre, and tunable bandwidth from 3 MHz to 20 MHz was designed in 65 nm CMOS technology. The layout occupies a silicon area of 0.172 mm². The filter uses a reduced-in-size resistor bank, which was designed according to the proposed calculation method for resistor's value. The simulation results coincide well with the initial requirements for bandwidth tuning range and accuracy. The designed filter achieves a PVT tuning range of 39 % with a maximum tune step size of 2 %. Integrated input-referred noise over the entire bandwidth varies from 50 μ V to 130 μ V, while the filter dissipated power is bandwidth dependent and varies from 13 mW to 23 mW when connected to a 1.2 V supply.

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