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# Simple Anti Capacitor Open-circuit Self-oscillation in a CMOS Schmitt trigger-invertor Oscillator circuit for a Fail-safe Relay Drive

***Abstract***. *Oscillator circuits with a CMOS Schmitt trigger-inverter are commonly used in applications that relate to relay driver circuits. It is possible to devise a fail-dangerous occurrence from the circuit, in which an open fault happens at the input circuit between the capacitor and input inverter IC. The causes of this self-oscillation event contribute to the failure of other parts of the circuit. This paper presents countermeasures for self-oscillation of the capacitor open-circuit self-oscillation in a CMOS Schmitt trigger-invertor oscillator circuit for a fail-safe relay drive. The proposed circuit replaces a normal 2-pin capacitor with a special 4-pin designed capacitor which connects a parallel resistor between the input CMOS inverter and the ground source. This paper carried out experimentation using Failure Modes and Effects Analysis (FMEA).The results showed that the output logic was high when the circuit had an open fault. Thus, the new designed circuit had no fail-dangerous occurrences.*

***Streszczenie.*** *W artykule opisano środki zaracze zapobiegające samooscylacjom w obwodzie pojemnościowym CMOS przerzutnika Schmitta w obwodzie przekształtnika. Metoda poleg ana zastąpieniu dwukońcówkowej pojemności obwodem z czterema końcówkami z rezystorem miedzy wejściem przekształtnika a masą.* ***Prosty układ kondensatora zapobiegający samooscylacjom w obwodzie przerzutnika Schmitta w układzie przekształtnika .***

**Keywords:** CMOS inverter, Self-oscillation, Open-fault, Fail-safe
**Słowa kluczowe:** przekształtnik CMOS, samooscylacje, przerzutnik Schmitta.

## Introduction

In the field of power electronics, especially motor drive systems, the motor current cut-off in terms of both fail-safe and cost-effectiveness is important because cut-off relays have additionally been provided and a driver circuit should be embedded in the motor drive control systems. Meanwhile, CPU-based safety-related control circuits are being utilised in the industry. However, such CPU-based safety-related control applications require certain subsidiary safety measures, e.g. diagnostic functions and redundant hardware structure, since their circuits are not simple. Moreover, CMOS elementary logic gates [1], which are widely used and easily available, are not normally applicable to safety-related controls because of the possibility of self-oscillation in the case of input open-faults. A key requirement of the safety relay drive circuit is no fail-dangerous occurrences when a fault occurs in the operation. The problem with such a circuit is self-oscillation (e.g. the input IC open-fault)[2]. The proposed relay drive circuit will be designed in the form of a fail-safe circuit [3] that does not use integrated circuits, a CPU, or complex systems. The paper [4-5] presents how to solve such problems by employing a special 4-pin designed capacitor covered by a metal shield between the input CMOS inverter and the ground source, which resolves the parasitic capacitance issue within the CMOS inverter. However, the solution could create a new problem where the capacitor or metal shield has an open-fault occurring spontaneously.

Fault diagnosis of the analogue circuit is an area of great importance in the design, manufacturing and utilisation processes for electronic devices. For diagnostic methods, there are two main causes of such situations. The first is the difficulty in diagnosing analogue circuits due to the non-linear characteristics and tolerances of the system's elements. The second is new challenges such as limited access to the system's interior. [6]. Safety analyses of newly-developed devices and systems are crucial to guaranteeing their safety. With regard to this fail-safe relay drive, IEC 61800-5-2:2007, adjustable speed electrical power drive systems, FMEA (Failure Modes and Effects Analysis) has been carried out, including being intentionally designed as a hardware-based component that is inherently safe.[7]

This paper presents the oscillator circuit by CMOS inverter IC for the fail-safe relay drive circuit. Specific safety measures of this proposed circuit, which can be solved by improving relaxation oscillator circuit, are provided by special capacitors 4-pin and resistor. The circuits can counteract self-oscillation, which capacitor input open-fault, feedback resistor is not connected to input, and add the input resistance to maintain the level of the input signal logic. To guarantee safety, FMEA (Failure Modes and Effects Analysis) has been carried out, including multi-failure modes, as it has been intentionally designed as a hardware-based component that is inherently safe.

## CMOS Schmitt trigger Inverter oscillator circuit and capacitor open-circuit self-oscillation

The countermeasures act against the CMOS self-oscillation with input open-fault in the oscillator circuit. It starts from the switching behaviour of the CMOS inverter, which can be achieved by study of the passive capacity and passive resistance. The equivalent circuit of CMOS inverter IC for consideration operation [8], when the input signal is operated at a low-level, the output is pulled through the PMOS device. When the input signal is operated at a high-level, the output is pulled through the NMOS to the ground. The stray capacitance between the junctions of the CMOS semiconductor structure as illustrated is shown in Figure 1.

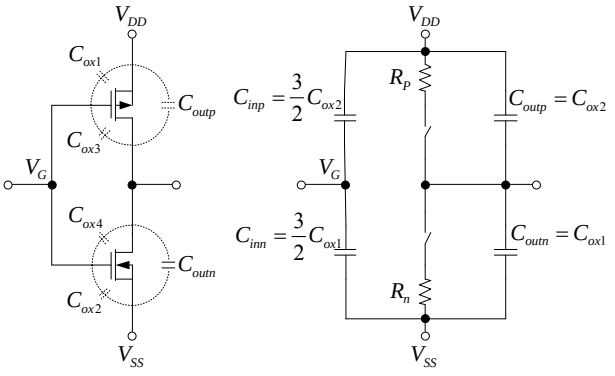



Fig.1. CMOS inverter schematic circuit with junction capacitance

Figures 2 and 3 show the findings of the voltage at the G point ($V_G$), of which the state is stable $C_{ox1}$=$C_{ox2}$, and where $C_{ox3}$ and $C_{ox4}$ are very low values that may then be neglected. The voltage drop at the G point is half the value of the voltage source ($V_{DD}$), while the output voltage swings from $V_{DD}$ to ground if this voltage is of higher value than the set-point operation of the MOSFET.

For the conditions of $Q_1$ active (on) and $Q_2$ not active (off), the voltage at the common G point ($V_G$) can be considered as equation (1) and the equivalent circuit, as shown in Figure 2.

$$V_G = \frac{\frac{1}{C_{ox2}}}{\frac{1}{C_{ox1}+(C_{ox3}+C_{ox4})}+\frac{1}{C_{ox2}}} V_{DD} \quad (1)$$

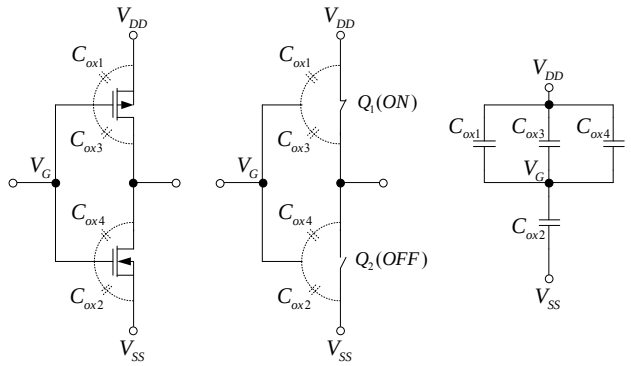



Fig.2. Equivalent circuit of Q1 active (on) and Q2 not active (off)

For the conditions of Q1 not active (off) and Q2 active (on), the voltage at the common point G (VG) can be considered as equation (2) and the equivalent circuit, as shown in Figure 3.

$$V_G = \frac{\frac{1}{C_{ox2}+(C_{ox3}+C_{ox4})}}{\frac{1}{C_{ox2}+(C_{ox3}+C_{ox4})}+\frac{1}{C_{ox1}}} V_{DD} \quad (2)$$

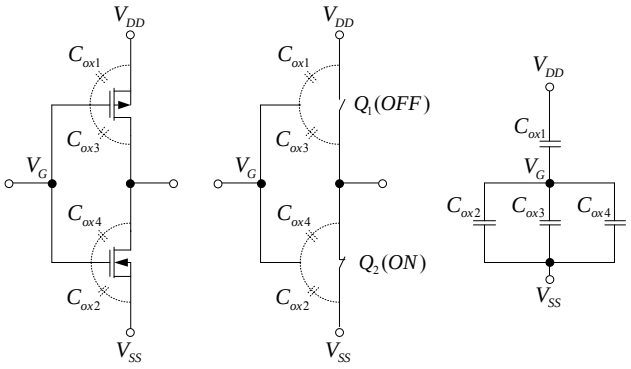
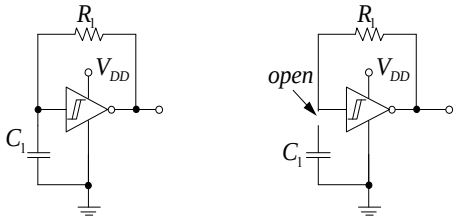



Fig.3. Equivalent circuit of Q1 not active (off) and Q2 active (on)

The basic CMOS inverter oscillator circuit is shown in Figure 4(a) with the period of the signal from the delay capacitor C1 of the charge and discharge cycles as well as the switching signals from the feedback resistor R1. The signal generator has a fail-dangerous, when the open input capacitor to the input of CMOS inverter, as shown in Figure 4(b). The circuit will have high-frequency self-oscillation as a result of capacitance value latent within itself with the capacity for about 5-10 pF. This high frequency signal is sent to a boost in the next section, which may cause the relay to drive unintentionally and fault with open input capacitor charge and discharge cycles.




a) Normal circuit b) Open fault circuit

Fig.4. CMOS Schmitt trigger-invertor oscillator circuit

Figure 5 shows the experimental results of an inverter with a Schmitt-trigger IC (74HC14) from the circuit in Figure 4(a) under normal operation frequency at 500 kHz. Figure 6 shows the self-oscillation effect under the open-circuit fault condition of the inverter IC from the circuit in Figure 4(b).

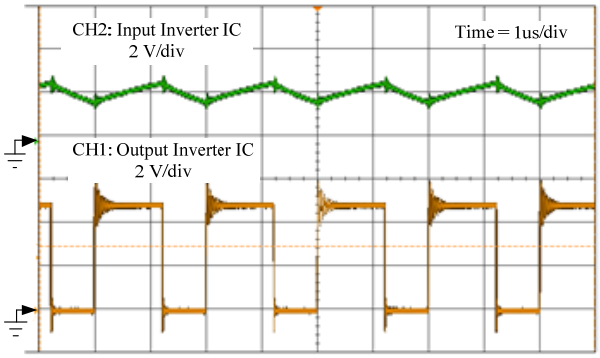



Fig.5. Experimental results of normal operation

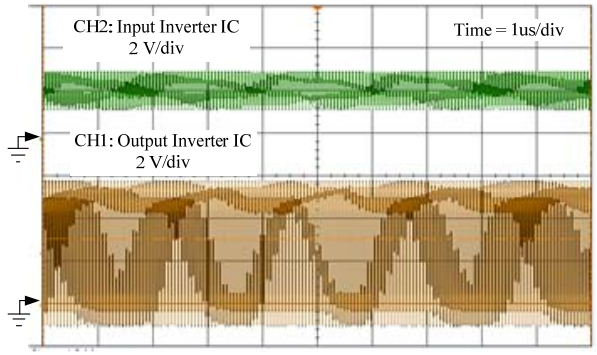
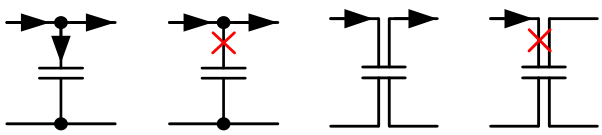



Fig.6. Experimental results of capacitor open-circuit fault

**Countermeasures against capacitor open-circuit self-oscillation**

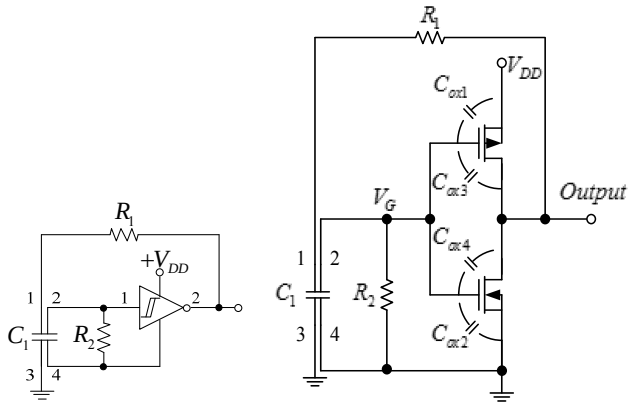
For the general capacitor, the junction doesn't separate from other parts of the circuit when an open-fault occurs at a pole. The current can still flow through a pole connection of the junction to the other part, which might be the system to fail-dangerous situation. For the fail-safe capacitor, the current cannot flow through to the other part when the open-fault occurs at a pole and cuts off the capacitor from the circuit. This system is a fail-safe situation.



a) General capacitor b) Fail-safe capacitor

Fig.7. Comparison of capacitors

The idea of this proposed circuit is countermeasure self-oscillation must be not a condition under the principle of Barkhausen stability criterion. For this method correction and improvement oscillator circuit, a special capacitor 4-pin is used to change the circuit when a capacitor open-fail feedback resistor is not connected to the input. The added input resistance maintains the level of the input signal logic, as shown in Figure 8.



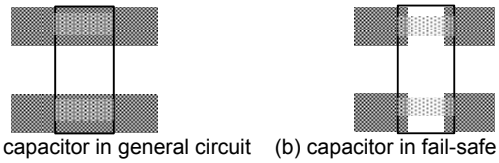

a) Normal circuit b) Equivalent circuit

Fig.8. The proposed circuit

Figure 8 presents an improved CMOS inverter relaxation oscillator circuit with 4-pin capacitor. The input of the circuit open fault will not cause a feedback resistor $R_1$ in series with the parasite capacitor. If $Q_1$ conducts and $Q_2$ does not conduct, feedback resistor $R_1$ does not connect to the VG point. The $Q_1$ does not conduct and $Q_2$ conducts the feedback resistor, which is not connected to the $V_G$ point either. The output will not cause self-oscillation with high-frequency.

Based on the conditions mentioned above, if no resistance is added in circuits, it could also be a cause of low-frequency self-oscillation when the resistor $R_2$ is added to the $V_G$ against the ground. The output signal is constant voltage from the power supply because the added resistance is greater than the sum of the resistance in the circuit.

The method presented above uses special capacitors that have four legs, which are rare or special order. In case special capacitors are unavailable, the design can be adapted for the PCB to use normal capacitors. This method cuts the copper on the PCB and uses the terminal of the capacitor instead.



(a) capacitor in general circuit (b) capacitor in fail-safe circuit

Fig.9. Comparison of capacitors in general and fail-safe circuits

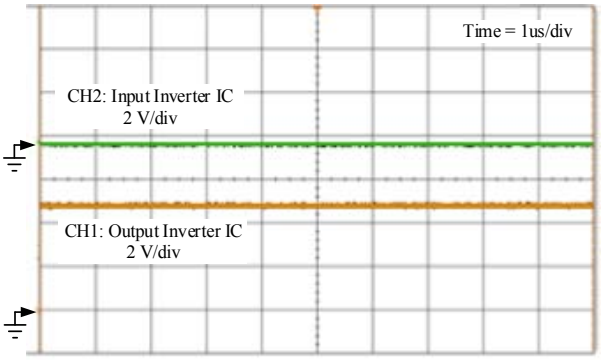



Fig.10. Experimental results of fail-safe capacitor open-circuit fault

The experimental circuit is used to verify that it was not self-oscillation that input capacitor open-fault. The circuit uses a 4-pin capacitor and the resistor applied between the G point and the S point under normal operation at 500 kHz input signal and open-circuit fault condition of inverter IC is considered. Self-oscillation does not appear in the case of an open-circuit fault with an inverter IC.

Safety analyses of newly-developed devices and systems are crucial to guarantee their safety. FMEA (Failure Modes and Effects Analysis) has been carried out, including multi-failure modes, as it is intentionally designed to be a hardware-based component with inherent safety. The FMEA analysis conditions are as follows: the fault model for ICs is the single-stuck-at model; IC pin stuck at the logic 0 or 1, as well as open fault. The fault of the hardware components is open, short or their value increases/decreases.

Table 1 shows the FMEA results of the failures in the oscillator circuit. For the result, the effects of output voltage failure Vout1 and Vout2 are the same when a failure occurs in any case in the oscillator circuit. For all failure cases, there were no significant consequences at output voltage. In the oscillator circuit, no fail-dangerous or effects occurred to other parts of the circuit according to the principle of fail-safe.

Table 1. FMEA of single failures in the oscillator circuit

| Device | | Failure mode | Effect of failure |
|---|---|---|---|
| $R_1$ | | $R_1$*0.5 | Change of circuit characteristic |
| | | $R_1$*2 | Change of circuit characteristic |
| | | Open | No output signal |
| | | Short | Change of circuit characteristic |
| $R_2$ | | $R_2$*0.5 | Change of circuit characteristic |
| | | $R_2$*2 | Change of circuit characteristic |
| | | Open | Change of circuit characteristic |
| | | Short | No output signal |
| $C_1$ | | $C_1$*0.5 | Change of circuit characteristic |
| | | $C_1$*2 | Change of circuit characteristic |
| | | Open Pin 1 | No output signal |
| | | Open Pin 2 | No output signal |
| | | Open Pin 3 | Normal output |
| | | Open Pin 4 | Normal output |
| | | Short | No output signal |
| IC 1 | pin1 | Struck at 1 | No output signal |
| | | Struck at 0 | No output signal |
| | | Open | Change of circuit characteristic |
| | pin2 | Struck at 1 | No output signal |
| | | Struck at 0 | No output signal |
| | | Open | No output signal |

**Conclusion**

This paper proposes a new anti-oscillation control based on an inherently safe design and FMEA (Failure Modes and Effects Analysis). The method uses a special capacitor and added resistor in considering the self-oscillation of CMOS. The effectiveness of the proposed method was confirmed using an experimental circuit. Moreover, methods using conventional capacitors by PCB solutions were also introduced. This proposed method has advantages over other methods because of the lack of need to add another device. The results of the work proposed can be added to the internal resistance of the integrated circuit in order to prevent the failure of the input resistors, which reduces the likelihood of failure for the input of the circuit.

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