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Realization of a Carrier-based Discontinuous SVPWM Technique for Two-Phase Four-Leg Voltage Source Inverter

Abstract. *This paper presents the carrier based discontinuous space vector pulse width modulation (DSVPWM) for two-phase four-leg voltage source inverters (VSI) fed resistive and inductive loads. This proposed technique is focused on the switching losses and output current ripple reduction in each phase-leg of inverter which does not depends on the lagging and leading power factor load. In addition, the carrier based DSVPWM is modified from conventional two-phase four-leg VSI by replacing the zero space vector in each switching sequence. This proposed discontinuous modulation strategy has 180 degrees for unmodulated region. Experimental results provide the performance comparison between the discontinuous SVPWM (DSVPWM) and the traditional continuous SVPWM (CSVPWM) techniques to confirm the reduction of switching losses and output current ripple at high modulation index. The experimental results show that total average values of normalized switching losses of the DSVPWM and the CSVPWM are 7.908 and 11.174, respectively in which the proposed DSVPWM can reduce the switching losses from the conventional CSVPWM up to 29 percent.*

Streszczenie. *W artykkule opisano nieciągła technikę modulacji szerokości impulsu DSVPWM zastosowaną w dwufazowych czterogałęźnym przekształtniku VSI obciążonym indukcyjnością i rezystancją. Projekt zakładał ograniczeniu strat przełączania i zafalowania prądu. Eksperymentalnie porównano zaprojektowany układ z tradycyjnym układem ciągłym.* ***Nieciągła technika modulacji szerokości impulsu DSVPWM zastosowana w dwufazowych czterogałęźnym przekształtniku VSI***

do Przeglądu Elektrotechnicznego *- polski tytuł na końcu streszczenia - Polish tittle at the end).*

Keywords: Two-phase four-leg inverter, Switching losses, Ripple current, Discontinuous space vector pulse width modulation.
Słowa kluczowe: przekształtnik dwufazowy, nieciągła modulacja szerokości impulsu DSVPWM.

■ Introduction

An increase of performance of the three-leg voltage source inverter can be enhanced by reducing the switching losses and output ripple current when the discontinuous space vector pulse width modulation (DSVPWM) technique for high modulation index has been performed [1-3]. Many types of DSVPWM techniques such as DPWMMIN, DPWMMAX, DPWM 0, DPWM 1 and DPWM 2 of three-phase voltage source inverters (VSIs) depend on types of power factor load. For example, DPWM 0 is suitable for a leading power factor load and DPWM 2 is fit for a lagging power factor load [4]. In addition, three-leg voltage source inverters can be applied to two-phase induction motor of both of the asymmetrical and symmetrical parameter types for industrial application [5]. Especially, the two-phase four-leg voltage source inverter fed two-phase motors drive has an advantage of a lower DC bus voltage requirement compared to the DC bus voltage of two-leg and three-leg VSI at the same output voltage of inverter [6]. On the other hand, a disadvantage of four-leg VSI is more number of switching devices than two and three-leg VSI. Therefore, to reduce the switching losses in switching devices in each leg, the modulating function of DSVPWM technique for two-phase four-leg inverter fed balanced R-L load is proposed in this study. The experimental results of a decrease of switching losses and output current ripples for the proposed DSVPWM modulation are compared with the conventional CSVPWM.

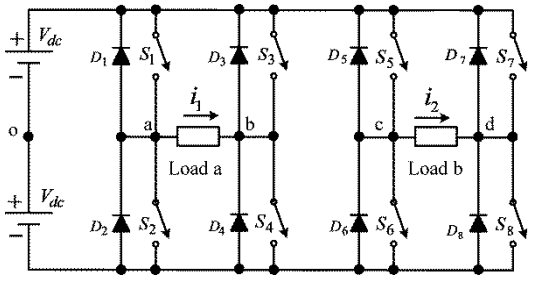


Fig. 1. A proposed two-phase four-leg voltage source inverter

Table 1. Switching state and corresponding active space vector

Space vector	Switching state		Space vector magnitude (V)	Location (Degrees)
$\overline{SV_0}$	0000	0011	0	Origin
$\overline{SV_1}$	1000	1011	$2V_{dc}$	0^0
$\overline{SV_2}$	1010	–	$\sqrt{2}(2V_{dc})$	45^0
$\overline{SV_3}$	0010	1110	$2V_{dc}$	90^0
$\overline{SV_4}$	0110	–	$\sqrt{2}(2V_{dc})$	135^0
$\overline{SV_5}$	0100	0111	$2V_{dc}$	180^0
$\overline{SV_6}$	0101	–	$\sqrt{2}(2V_{dc})$	225^0
$\overline{SV_7}$	0001	1101	$2V_{dc}$	270^0
$\overline{SV_8}$	1001	–	$\sqrt{2}(2V_{dc})$	315^0
$\overline{SV_9}$	1111	1100	0	Origin

■ Two-phase four-leg SVPWM technique

A main circuit of the two-phase four-leg voltage source inverter (VSI) connected to the balanced R-L loads shows in Fig.1.

The terminal voltages, v_{ao} , v_{bo} , v_{co} and v_{do} are phase voltages and the line terminal voltages, v_{ab} and v_{cd} are connected to the balanced R-L loads. The main power circuit has 8 switching devices and 16 switching states which consist of 12 active voltage vectors and 4 null vectors as shown in Table 1. For switching states in Table 1, there are eight possible voltage vectors $\left(\overline{SV_1}, \overline{SV_2}, ..., \overline{SV_8}\right)$ and two null vectors $\left(\overline{SV_0}(0000)\right)$ and $\left(\overline{SV}(1111)\right)$. In the switching states, upper and lower switches assigned with “1” or “0” mean to turn-on and turn-

off, respectively. Four active vectors $\left(\overline{SV_1},\overline{SV_3},\overline{SV_5},\overline{SV_7}\right)$ have the length of $2V_{dc}$ and four active vectors $\left(\overline{SV_2},\overline{SV_4}\overline{SV_6},\overline{SV_8}\right)$ have the length of $\sqrt{2}\left(2V_{dc}\right)$, unlike the SVPWM analysis of three-phase VSI which has the same magnitude active voltage vector of each sector [3]. Fig. 2 shows the arbitrary output voltage and the location of active space vectors in a d-q plane which is divided into 8 sectors with 45 degrees. Due to the similar principle to the conventional two-phase four-leg SVPWM [7], mathematical calculation of switching times for the two-phase four-leg SVPWM method can be dealt with in the same manner as for the conventional one. The desired output voltage $\overline{V_o^*}$ in vector form which is a rotating vector can be calculated in terms of the average of a number of these space vectors within a switching period in each sector as follows

(1) $$\overline{V_0^*}=V_0\angle\theta=\frac{T_{U1}}{\Delta T/2}\overline{U_1}+\frac{T_{U2}}{\Delta T/2}\overline{U_2}$$

(2) where $$\frac{\Delta T}{2}=T_{U1}+T_{U2}+T_{SV0}+T_{SV9}$$

$\overline{U_1}$ and $\overline{U_2}$ are two basic adjacent vectors; θ is sampled angular position; T_{U1}, T_{U2} are active times for the two basic adjacent vectors; T_{SV0}, T_{SV9} are times for null vectors; and ΔT is a carrier period. Generally, for a symmetrical space vector pattern, space vector time for each zero switching state (T_{SV0}, T_{SV9}) is set to be equal.

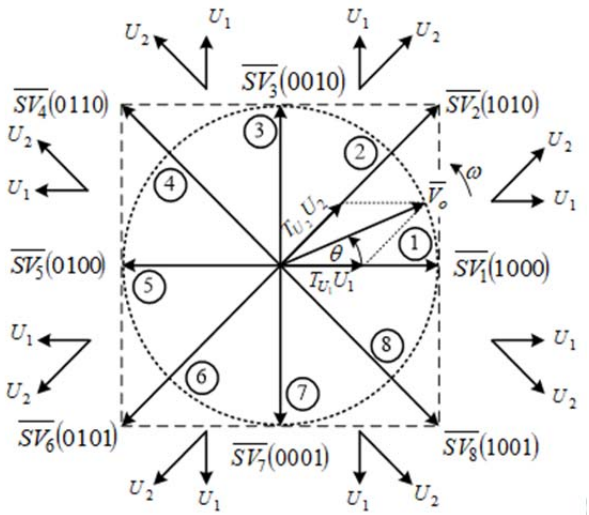


Fig. 2. Location of active space vectors in d-q plane and arbitrary output voltage.

From Eq. (1), an example of the relationship between the space vector active times at different angles between 0 and 180 degrees divided into the equal four sectors (sector 1 to sector 4) can be determined by the equations in Table 2. These equations can be used for deriving the phase-leg reference voltage waveforms for CSVPWM. An example for calculating and drawing the phase-leg reference voltage of sector 1 for angles between 0 and 45 degrees are started from the equation below

(3) $$\frac{T_{SV_1}}{\Delta T/2}=\frac{M}{\sqrt{2}}\sin\left(\frac{\pi}{4}-\theta\right)$$

(4) $$\frac{T_{SV_2}}{\Delta T/2}=\frac{M}{2}\sin\theta$$

As illustrated in Fig. 2, the maximum possible magnitude of the output voltage vector is $2V_{dc}$ and the Locus voltage is a circular path; therefore, the output voltage vector, V_o^* can be expressed by

(5) $$V_o^*=\frac{T_{SV_1}}{\Delta T/2}\left(\overline{SV_1}\right)$$

Substituting Eq. (3) and $\overline{SV_1}=2V_{dc}$ into Eq. (5) and when $\theta=0$ degree, the magnitude of output voltage can be given by

(6) $$V_o^*=MV_{dc}\qquad\text{(Peak voltage)}$$

where M is the modulation index in range of $0\le M\le 2$.

Then, the phase-leg reference voltage or equivalent voltage in average values for four phase-leg reference voltage with respect to the midpoint of DC bus voltage over the time interval $\Delta T/2$ of sector 1 can be written as

(7) $$\frac{v_{ao}}{V_{dc}}=\frac{M}{\sqrt{2}}\left[\sin\left(\frac{\pi}{4}-\theta\right)+\frac{1}{\sqrt{2}}\sin\theta\right]$$

(8) $$\frac{v_{bo}}{V_{dc}}=\frac{-M}{\sqrt{2}}\left[\sin\left(\frac{\pi}{4}-\theta\right)+\frac{1}{\sqrt{2}}\sin\theta\right]$$

(9) $$\frac{v_{co}}{V_{dc}}=\frac{M}{\sqrt{2}}\left[\frac{1}{\sqrt{2}}\sin\theta-\sin\left(\frac{\pi}{4}-\theta\right)\right]$$

(10) $$\frac{v_{do}}{V_{dc}}=\frac{-M}{\sqrt{2}}\left[\sin\left(\frac{\pi}{4}-\theta\right)+\frac{1}{\sqrt{2}}\sin\theta\right]$$

Table 2. Switching times

Sectors	Angular position	Switching times
Sector 1	$0^0<\theta<45^0$	$\frac{T_{SV_1}}{\Delta T/2}=\frac{M}{\sqrt{2}}\sin\left(\pi/4-\theta\right)$ $\frac{T_{SV_2}}{\Delta T/2}=\frac{M}{2}\sin\left(\theta\right)$
Sector 2	$45^0<\theta<90^0$	$\frac{T_{SV_2}}{\Delta T/2}=\frac{M}{2}\sin\left(\pi/2-\theta\right)$ $\frac{T_{SV_3}}{\Delta T/2}=\frac{M}{\sqrt{2}}\sin\left(\theta-\pi/4\right)$
Sector 3	$90^0<\theta<135^0$	$\frac{T_{SV_3}}{\Delta T/2}=\frac{M}{\sqrt{2}}\sin\left(3\pi/4-\theta\right)$ $\frac{T_{SV_4}}{\Delta T/2}=\frac{M}{2}\sin\left(\theta-\pi/2\right)$
Sector 4	$135^0<\theta<180^0$	$\frac{T_{SV_4}}{\Delta T/2}=\frac{M}{2}\sin\left(\pi-\theta\right)$ $\frac{T_{SV_5}}{\Delta T/2}=\frac{M}{\sqrt{2}}\sin\left(\theta-3\pi/4\right)$

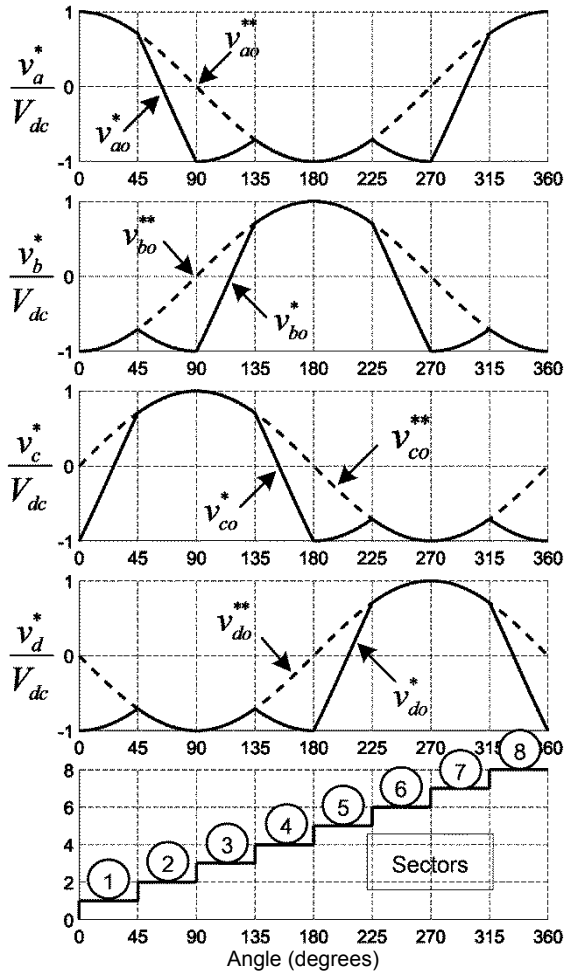


Fig. 3. Phase-leg reference voltage waveforms for CSVPWM

As described before, the phase-leg reference voltage of 8 sectors can also be calculated and the phase-leg reference voltage waveforms as the function of angle for 0 to 360 degrees can be drawn as shown in Fig. 3, where v_{ao}^{**}, v_{bo}^{**}, v_{co}^{**} and v_{do}^{**} are fundamental of phase-leg reference voltage, and v_{ao}^{*}, v_{bo}^{*}, v_{co}^{*} and v_{do}^{*} are phase-leg reference voltage. These phase-leg reference voltage are compared with the carrier waveform to generate the gate driver signals.

■ **Proposed DSVPWM**

The principle of carrier based CSVPWM for the two-phase four-leg VSI discussed earlier can be modified as discontinuous pulse or discontinuous modulation. A main purpose of using the DSVPWM is to reduce the switching losses and output current ripple at high modulation index. This DSVPWM is carried out by alternating the null voltage vectors $\overline{SV}_0$ and $\overline{SV}_9$. In this paper, the modulating function is calculated using only null voltage vector $\overline{SV}_0$ as shown in Fig. 4. According to Fig. 4 which presents the pulse pattern and phase-leg reference voltage for the sector 1 only, an example of calculating the phase-leg reference voltages, v_{ao} in average values over the time interval $\Delta T/2$ of sector 1 can be determined by

$$v_{ao} = V_{dc}\left[\frac{T_{SV1}}{\Delta T/2} + \frac{T_{SV2}}{\Delta T/2} - \frac{T_{SV0}}{\Delta T/2}\right] \tag{11}$$

where T_{SV0}, T_{SV1}, and T_{SV2} are the switching time sequencing in a half period of switching for sector 1 and

$$T_{SV0} = \frac{\Delta T}{2} - T_{SV1} - T_{SV2}.$$

After substituting the T_{SV0} into Eq. (11) gives

$$v_{ao} = 2V_{dc}\left[\frac{T_{SV1}}{\Delta T/2} + \frac{T_{SV2}}{\Delta T/2} - \frac{1}{2}\right] \tag{12}$$

The other three reference phase-leg voltages can also be calculated as described before and then gives

$$v_{bo} = -V_{dc} \tag{13}$$

$$v_{co} = 2V_{dc}\left[\frac{T_{SV2}}{\Delta T/2} - \frac{1}{2}\right] \tag{14}$$

$$v_{do} = -V_{dc} \tag{15}$$

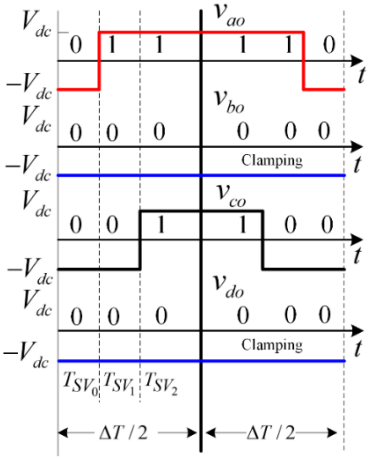


Fig. 4. Pulse pattern and phase-leg reference voltage for the sector 1

To calculate the phase-leg reference voltage as a function of θ and M for DSVPWM by substituting both of Eqs. (3) and (4) into Eq. (12) and Eq. (14) based on the midpoint of the DC bus voltage, for sector 1 only, the v_{ao}/V_{dc} and the v_{co}/V_{dc} can be derived whereas the v_{bo}/V_{dc} and the v_{do}/V_{dc} are constant as expressed below

$$\frac{v_{ao}}{V_{dc}} = \sqrt{2}M\sin\left(\frac{\pi}{4} - \theta\right) + M\sin\theta - 1 \tag{16}$$

$$\frac{v_{bo}}{V_{dc}} = -1 \tag{17}$$

$$\frac{v_{co}}{V_{dc}} = M\sin\theta - 1 \tag{18}$$

$$\frac{v_{do}}{V_{dc}} = -1 \tag{19}$$

After calculating like the approach described before, the four phase-leg reference voltage of DSVPMW for all 8 sectors can be plotted as demonstrated in Fig. 5.

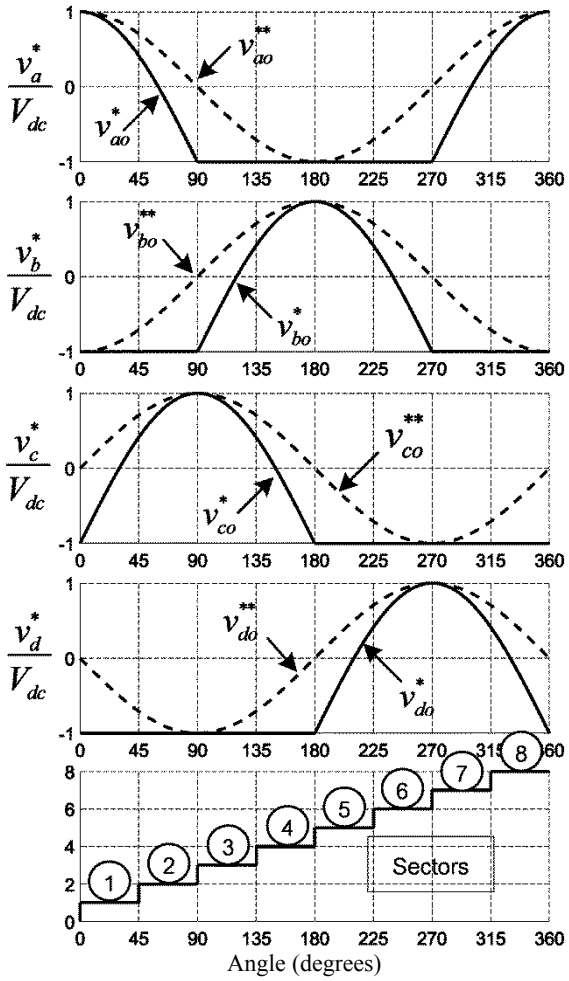


Fig. 5. Phase-leg reference voltage waveforms for proposed DSVPWM

■ Switching loss analysis

The switching losses and output current ripple of both CSVPWM and DSVPWM are compared while the conduction losses is neglected because the conduction losses of both methods are insignificant in term of the modulation index and the switching frequency variation [8]. Fig. 6(a) shows one-leg voltage source inverter circuit. Fig. 6(b) shows the gate driver signal, the voltage across terminals of switching device, the current flowing through switching device S1 and the average power switching losses for switching device S1.

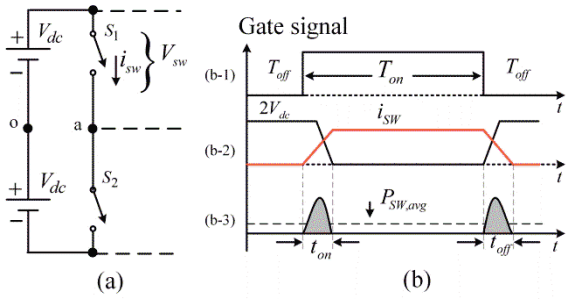


Fig. 6. Switching loss characteristics (a) one-leg inverter power circuit (b) Linearized switching characteristics (b-1) gate driver signal (b-2) voltage cross switching and load current flowing through switching device S_1 (b-3) average switching power loss.

The switching power loss during turn-on and turn-off time process is previously proposed [9]. Total average switching loss in a switch period can be expressed as

$$P_{sw,loss} = P_{on,avg} + P_{off,avg} \tag{20}$$

$$P_{sw,loss} = f_{sw} I_{sw} \left(t_{on} + t_{off}\right) \frac{V_{dc}}{3} \tag{21}$$

The power switching loss, $P_{sw,loss}$ depends on the switching frequency, f_{sw} and the load current, I_{sw}. The switching frequency of the proposed DSVPWM method is 1.5 times of the CSVPWM method; therefore, values of the switching frequency of the CSVPWM and the proposed DSVPWM method are 2kHz and 3kHz, respectively. For the normalized switching loss analysis, the normalized switching loss waveform for CSVPWM is similar to the absolute load current $|I_{sw}|$ while the normalized switching loss for the DSVPWM method is 1.5 times of $|I_{sw}|$ and zero at the clamping zone resulting in a reduction in switching losses.

■ Experimental results

Figs. 7 and 8 show the proposed system and the experimental setup consisting of a single rectifier providing 300V_{DC}, a four-leg VSI, and the balanced two-phase R-L loads. Each R-L load has resistance of 59 Ω and 50mH.

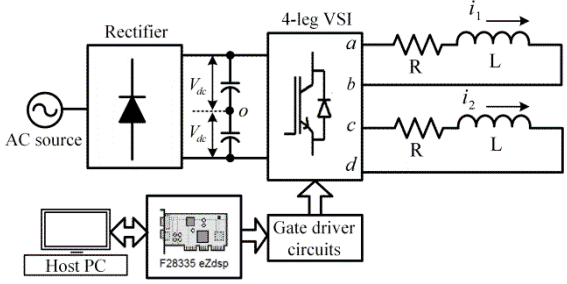


Fig. 7. A proposed two-phase four-leg VSI system

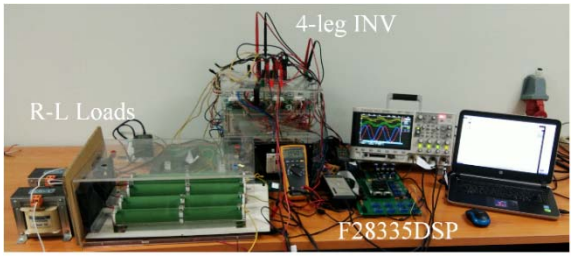


Fig. 8. Experimental setup for two-phase four-leg VSI system

The modulated signals for driving all IGBTs are generated by the TMS320F28335 DSP board with MATLAB/Simulink. An algorithm of MATLAB/Simulink for the proposed DSVPWM is shown in Fig. 9; the fundamental frequency of output voltage and a sampling time are defined as 50Hz and 100 μs by Ramp generation block set, and the maximum modulation index is set at 2. The PWM signals are established by ePWM1- ePWM4 modules at the switching frequency of 2kHz for CSVPWM and of 3kHz for DSVPWM. For DAC converters, ePWM5 and ePWM6 are applied as DACs by applying PWM signals through low pass filters to be displayed by a digital oscilloscope..

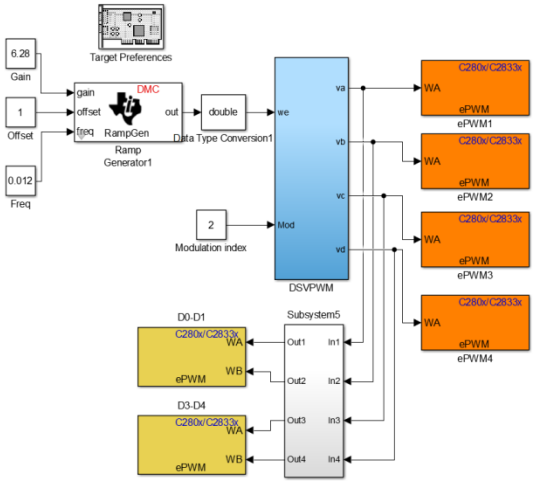


Fig. 9. MATLAB/Simulink for Algorithm development

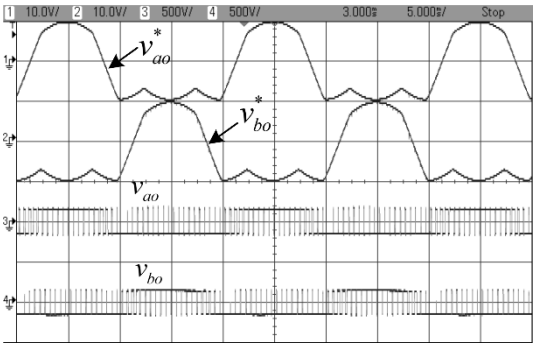
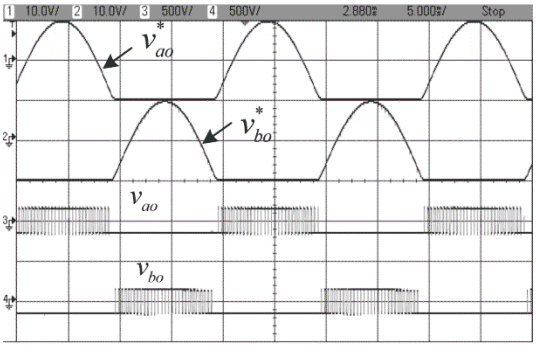
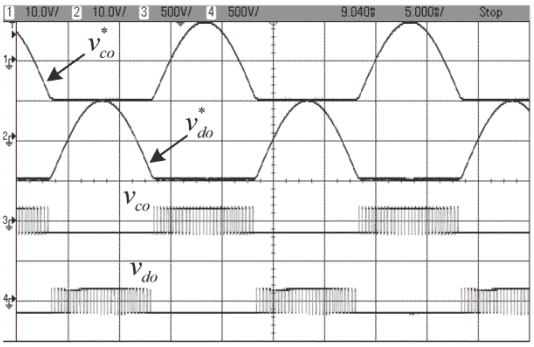


Fig. 10. CSVPWM (a) four phase-leg reference voltage of v_{ao}^* , v_{bo}^* and output phase voltage of v_{ao} , v_{bo} .



(a)



(b)

Fig. 11. Proposed DSVPWM (a) phase-leg reference voltage of v_{ao}^* , v_{bo}^* and output phase voltage of v_{ao} , v_{bo} (b) phase-leg reference voltage of v_{co}^* , v_{do}^* and output phase voltage of v_{co} , v_{do} .

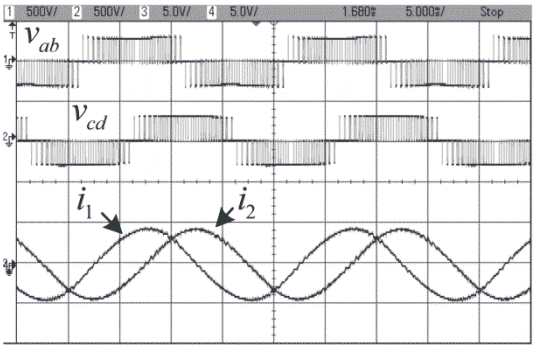


Fig. 12. Output voltage v_{ab} and v_{cd} , output current i_1 and i_2 of CSVPWM.

The test conditions are to compare the switching losses and the output load current ripple, i_1 and i , of the proposed DSVPWM and the conventional CSVPWM when the modulation index of both methods is fixed at 2. Fig. 10 shows the modulation waveforms of the conventional CSVPWM at which the phase-leg reference voltage of v_{ao}^* , v_{bo}^* and the output phase voltages of v_{ao} , v_{bo} are presented

Fig. 11 illustrates the modulation waveforms of the proposed DSVPWM and it is noted that the output pulse waveforms of each phase voltage of v_{ao} , v_{bo} , v_{co} and v_{do} does not switch at clamping zone owing to an unmodulated time. This clamping time leads to decrease the switching losses. Figs. 12 and 13 show the output voltages of v_{ab} and v_{cd} and the output current waveforms, i_1 and i_2 with the phase difference of 90 degrees for the conventional CSVPWM and the proposed DSVPWM, respectively.

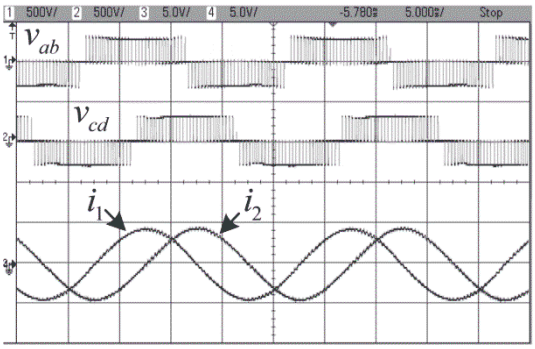


Fig. 13. Output voltage v_{ab} and v_{cd} , output current i_1 and i_2 of DSVPWM.

To compare the switching losses, Figs. 14 and 15 represent an analysis of normalized switching losses of the CSVPWM and the proposed DSVPWM, respectively. The voltages and currents are measured for mathematically calculating using MATLAB/Simulink. Fig. 14 demonstrates the normalized switching losses of the CSVPWM in each phase-leg derived by Eq. (21) when the carrier frequency of CSVPWM is 2 kHz, and absolute load current $|i_1|$ is representative of the normalized switching losses in switching devices, S1 and S2. The average values of normalized switching losses for CSVPWM of phase-leg *a*, *b*, *c* and *d* are 2.822, 2.822, 2.735 and 2.735 as shown in Figs. 4 (a) – (d), respectively. Fig. 15 illustrates the normalized switching losses of the proposed DSVPWM in each phase-leg calculated by Eq. (21) when the carrier

frequency of DSVPWM is fixed at 3 kHz, and 1.5times of absolute load current $|i_1|$ is representative of the normalized switching losses in switching devices, S1 and S2. The average values of normalized switching losses for DSVPWM of phase-leg *a*, *b*, *c* and *d* are 1.994, 1.904, 2.018 and 1.992 as shown in Fig. 15 (a) – (d), respectively. Table 2 summarizes the average values of the switching losses of CSVPWM and DSVPWM. A summation of switching losses of four legs of the DSVPWM method is minimum.

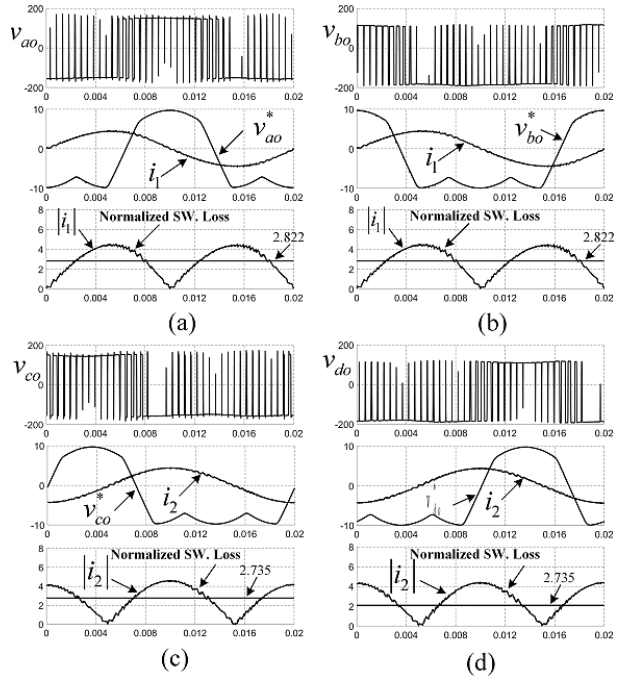


Fig. 14. Normalized switching losses of CSVPWM in each phase-leg.

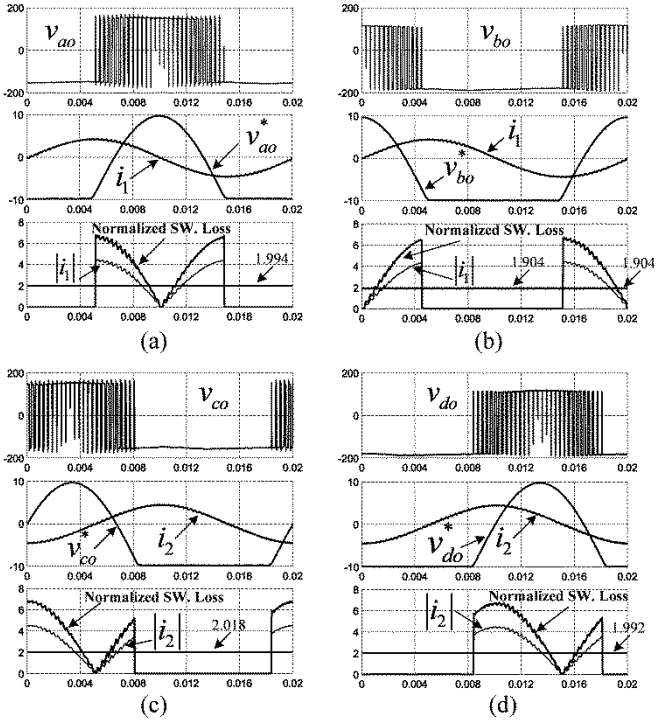


Fig. 15. Normalized switching losses of proposed DSVPWM in each phase-leg.

Table 3 Normalized switching losses

Method	Leg a	Leg b	Leg c	Leg d	Total
CSVPWM	2.822	2.822	2.735	2.735	11.174
DSVPWM	1.994	1.904	2.018	1.992	7.908
Reducing	29.34%	34.93%	26.20%	27.16%	29.22%

To compare the output current ripple analysis, the load current ripple waveforms of i_1 and i_2 for the CSVPWM method and the proposed DSVPWM method are shown in Fig. 16(a) and Fig. 16(b), respectively. The proposed ripple currents are not included the fundamental component using MATLAB/Simulink. The results show that the proposed DSVPWM is lower output current ripple than the conventional CSVPWM. Table 3 shows a comparison of the mean square values of load currents for CSVPWM and DSVPWM methods. It can be concluded that the mean square values of load currents of the proposed DSVPWM is lower than that of the conventional CSVPWM.

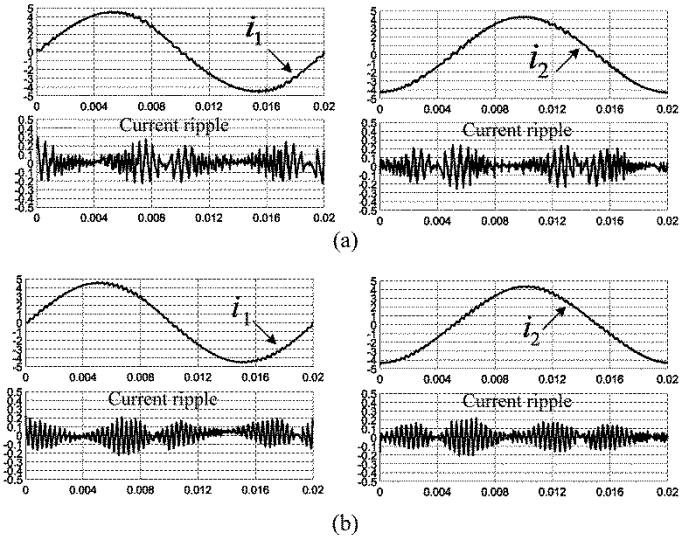


Fig. 16. Measured load current ripple (a) CSVPWM and (b) proposed DSVPWM

Table 4 comparison of mean square value of current ripples

Method	Load current	Mean square value
CSVPWM	i_1	$3.75e^{-3}$
	i_2	$5.03e^{-3}$
DSVPWM	i_1	$3.35e^{-3}$
	i_2	$4.69e^{-3}$

■ Conclusions

The discontinuous SVPWM (DSVPWM) technique compared with conventional CSVPWM for reducing the switching losses and output current ripple at high modulation index is investigated in this study. The experimental results confirm that the DSVPWM technique can reduce the switching losses up to 29% comparing with the CSVPWM. The reduction of switching losses is not depended on lagging or leading power factor. In addition, the proposed DSVPWM technique can be applied to drive the two-phase motor.

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