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doi:10.15199/48.2021.07.04

Design and Implementation of Parallel Multiplier Using Two Split Circuits

Abstract. *A novel binary parallel multiplier circuit is designed and implemented in this study. The proposed multiplier is a combination of two split circuits, namely, truncated multiplier and least-significant bit (LSB) circuit. The LSB multiplier is designed based on the Vedic mathematic expression, but some modification is made for it to be compatible with the truncated multiplier and to achieve correct results for all the multiplication values. The designed circuit is coded by the Verilog hardware description language (HDL) using Quartus II. The register transfer level is verified, and the gate level is simulated using the Cyclone IV field programmable gate array (FPGA) platform. The proposed multiplier operates at 107.5 MHz frequency operating speed and requires 155 combinational logics. Comparison with other reported works shows that the proposed design has 19.5% less delay time. The new parallel multiplier is suitable for applications in various electronic devices due to its good feature.*

Streszczenie. *W tym badaniu zaprojektowano i wdrożono nowatorski binarny równoległy obwód powielający. Proponowany mnożnik jest połączeniem dwóch oddzielnych obwodów, a mianowicie obwodu mnożnika obciętego i obwodu najmniej znaczącego bitu (LSB). Mnożnik LSB został zaprojektowany w oparciu o matematyczne wyrażenie wedyjskie, ale wprowadzono pewne modyfikacje, aby był zgodny z mnożnikiem obciętym i aby uzyskać poprawne wyniki dla wszystkich wartości mnożenia. Zaprojektowany obwód jest kodowany w języku opisu sprzętu Verilog (HDL) przy użyciu Quartus II. Poziom transferu rejestrów jest weryfikowany, a poziom bramki jest symulowany przy użyciu platformy programowalnej macierzy bramek (FPGA) Cyclone IV. Proponowany mnożnik działa przy częstotliwości roboczej 107,5 MHz i wymaga 155 logik kombinacyjnych. Porównanie z innymi zgłoszonymi pracami pokazuje, że proponowany projekt ma 19,5% krótszy czas opóźnienia. Nowy powielacz równoległy nadaje się do zastosowań w różnych urządzeniach elektronicznych ze względu na swoją dobrą funkcję. (**Projektowanie i implementacja równoległego mnożnika przy użyciu dwóch obwodów rozdzielonych**)*

Keywords: Parallel Multiplier, truncated multiplier, LSB multiplier, Vedic expression.
Słowa kluczowe: mnożnik, LSB – najmniej znaczący bit, równoległy obwód mnożący.

Introduction

The growing demand for portable devices and electronic systems that consist of digital circuits, such multipliers, counters, and adders, has forced designers to improve the performance of multiplier properties by improving the size area and reducing power consumption. Various methods have been utilized to enhance multiplier performance. The Booth algorithm requires the multiplication of two binary numbers in two's complement and shifts the result to a partial product [1-4]. L. P. Rubinfield [5] modified this algorithm for it to be able to multiply three signed binary bits at a time.

The array multiplier is a classic method involving the repeated addition of multiplying the multiplicand with the multiplier [6-9], shifting the partial product, then adding. The most frequently used technique is the Wallace tree multiplier, which was first devised by Chris. Wallace [10], It is a long-term technique that begins with the multiplication of two integer numbers [11-13] (it was later modified in [14]), reduction of the number of partial products, and addition by the adder.

A Vedic expression is a useful Indian mathematical method based on 16-word formulas for rapid mathematical operations [15-17]. The vertical and crosswise Vedic algorithm is one of the formulas used in designing multiplier circuits. The binary coded decimal technique was applied in [18] to design the multiplier by using a 3×3 multiplier circuit for accomplishing the desired multiplier bit number.

Multiplier applications are adopted in digital signal processing devices and multimedia equipment that require relative accuracy. Truncated multipliers can offer significant improvements in the terms of time, power, and area [19-21].

This research presents a novel multiplier design that is based on the combination of two separate circuits, namely, the truncated multiplier as the most significant bit (MSB) circuit and the least-significant bit (LSB) multiplier circuit.

The paper is organized as follows. The abstract of the work and the introduction of previous studies related to this one are presented in Section 1. A detailed explanation of the proposed multiplier circuit is shown in Section 2. The designed circuit is coded using hardware description language (HDL), synthesized, verified, and implemented in Section 3. The conclusions are presented in Section 4, followed by the references.

Proposed Design Circuit

The architecture of the N × N binary array multiplier circuit is defined as multiple repeated layers of binary addition to perform the multiplication of the multiplicand with the multiplier and obtain the partial product by using a group of AND logic gates and full adders. The binary array multiplier consists of multiple stages of adders as shown in Fig. 1. Hence, the carry-out value of the full adder circuit passes out through three logic gates, and the N × N binary multiplier requires 2N+1 gate delay time.

The repeated layers of the conventional multiplier circuit increase the propagation delay time to make it proportional to the growing N binary bits. For the 8 × 8-bit multiplier, the critical delay time is 17 gate delays.

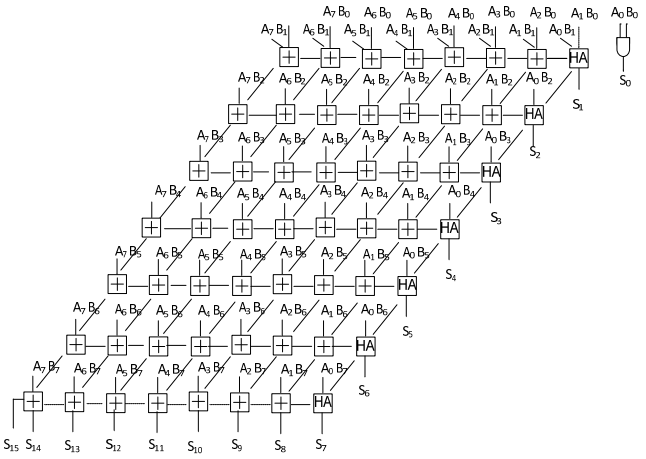


Fig.1. Conventional 8×8 -bit binary array multiplier circuit

To avoid the worst growing path delay time of the multiplier circuit, the presented 8×8 binary parallel multiplier design is equipped with two separate circuits: the truncated multiplier as a suitable fixed-width circuit to provide the MSB values and the high-speed multiplier as a second circuit for obtaining the LSB binary bits. The combination of truncated and LSB multipliers in the proposed design can reduce the propagation delay because the LSB output values passes through six steps, while the truncated multiplier delay is calculated to be half of that of the classic multiplier circuit with one more gate delay. Given that the two parts of the proposed design are processed sequentially, the total gate delay represents the propagation delay of the truncated multipliers (i.e., equal to 9 gate delays).

The basic idea of the proposed design is to use the truncated multiplier to prepare the MSB bits, and the other circuit is designed based on the Vedic mathematic expression (Fig. 2). Figure 2 shows how to use the 2×2 circuit to devise the first 2×4 circuit; in the same way, the second 2×4 circuit is prepared.

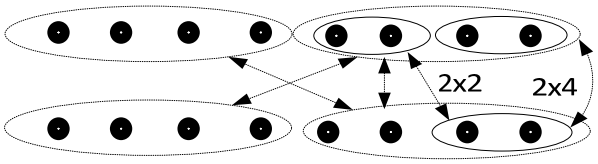


Fig.2. Vedic mathematic expression for 2×2 and the 2×4 circuits

As an above explained, the proposed 8×8 LSB multiplier circuit is designed based on Vedic expression. It is formatted as a two 4×4 sections. The first 4×4 circuit diagram is prepared to be a combination of pair of 2×4 circuits, and each of these circuits is designed based on 2×2 multiplier circuits. Taking into account the requires of shifting two bits to the left as shown in Fig. 3.

The 4×4 circuit diagram is used to provide the crossing Vedic expression based on Figure1. Hence the LSB section of the proposed 8×8 multiplier is limited by 8 digit bits, the crossing 4×4 circuit diagram is simplified to reduce the complexity of logic gates while preserving the correct values as in Fig. 4.

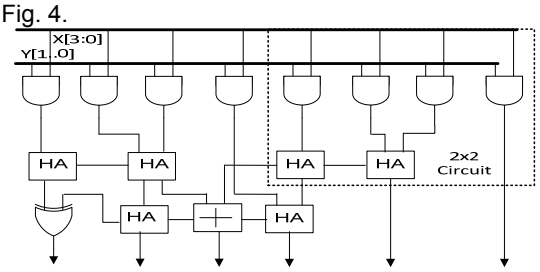


Fig. 3. The 2x4 circuit diagram

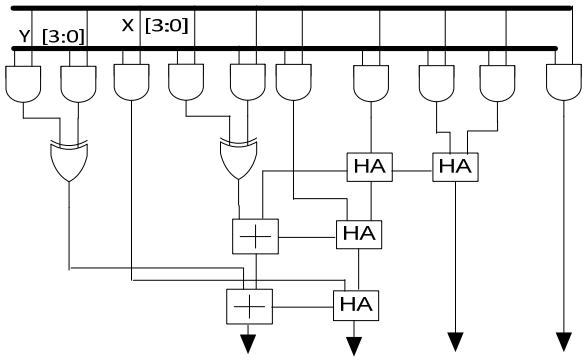


Fig. 4. Simplified 4x4 circuit diagram

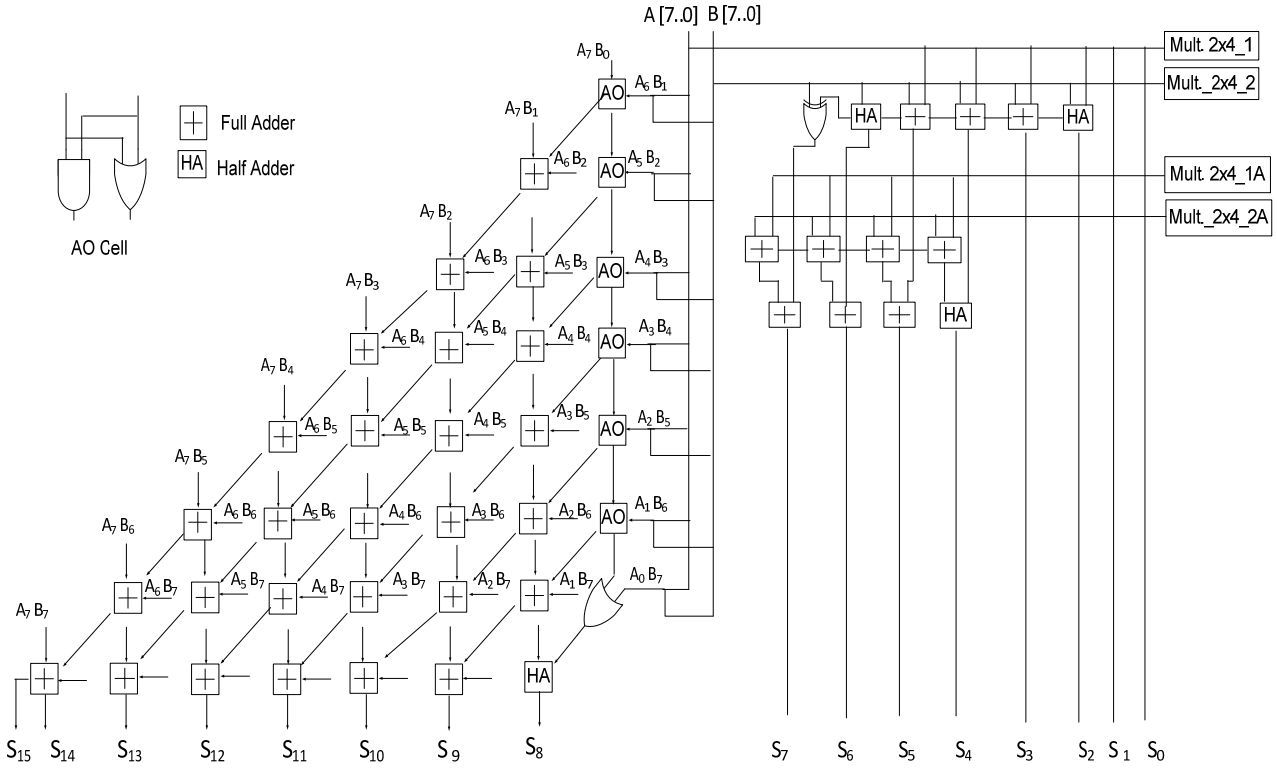


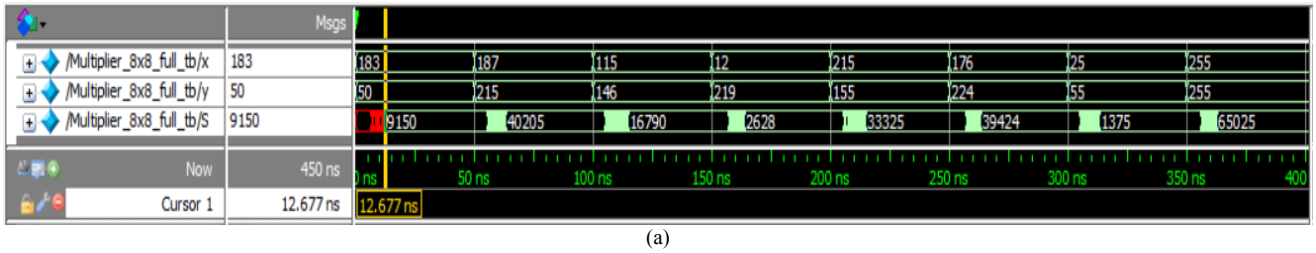
Fig. 5. An 8×8 parallel multiplier circuit diagram using truncated and the LSB multiplier circuits

The complete circuit diagram of the proposed two split 8x8 multiplier circuit, an 8x8 truncated multiplier circuit and the explained LSB multiplier circuit is compiled in one circuit diagram as in Figure 5.

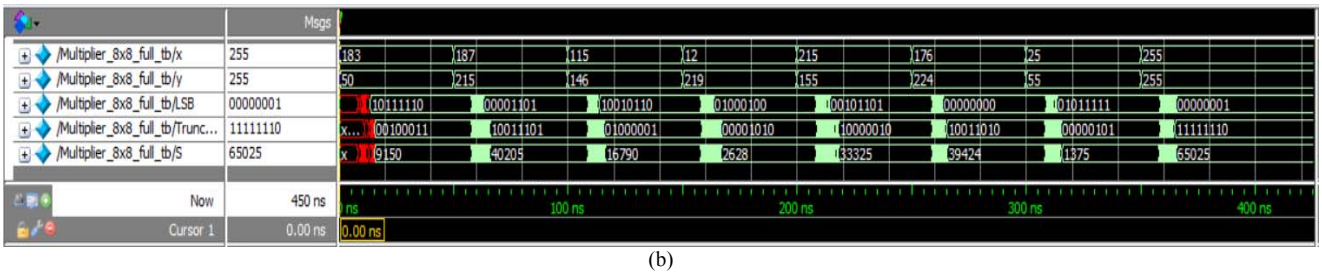
The wright part of the figure shows the architecture of the LSB multiplier circuit. A couple circuits of each of the 2×4 and the simplified 4×4 circuit are managed together. Three summation steps include half and full adders are used to obtain the desired circuit. Taking into account the requires of two and four shifting bits to the left in the first and second summation steps respectively.

Results and Discussions

The proposed multiplier is coded using Verilog HDL to simulate the designed parallel multiplier and check the validity of the circuit. Initially, the designed 2×4 circuits and the simplified 4×4 ones are coded using Verilog language and verified to prove the correctness of the results. Then, the complete designed circuits of the truncated and LSB multipliers (including the 2×4 and 4×4 circuits) are combined (Figure 4) for verification using Quartus II software. Gate level simulation of the proposed design is conducted using the Cyclone IV FPGA kit. The simulation result is shown in Figure 6 (a and b). The figure presents multiple x and y values, namely, output result (S) of each multiplication instance of x and y values. The achieved results are in agreement with those of the arithmetic multiplication. The vertical yellow line in Figure 6-a indicates that the required delay time to obtain the first multiplication result at an operating speed of 107.06 MHZ is 12.67 nanoseconds (NS). In addition to the x and y inputs and the S output values, other output fields are added in Figure 6-b to separately indicate the results of binary bit values of the LSB and truncated multiplier circuits.



(a)



(b)

Fig.5. Gate level simulation results. (a) Parallel multiplier output and (b) LSB, truncated, and S circuit throughput (a and b}

Table 1. A comparison of the designed parallel multiplier with a conventional multiplier and other previous works

8x8 parallel	This work	Conventional	[22]	[23]	[24]	[25]	[26]	[15]
FPGA kit	Cyclone IV EP4CGX15BF14C 6	Cyclone IV EP4CGX15BF14C 6	Virtex-4: XC4VSX35	Spartan-6: XC6SLX150T	NA	Virtex-4: XC4VLX15	NA	NA
Time Delay (NS)	12.67	15.6	13.87	23.67	20.2	15.2	28.99	24.1 6

A comparison of the designed parallel multiplier with a conventional multiplier and other previous works is shown in Table 1.

The comparison table shows multiple design of 8×8 binary multiplier using various method and techniques. The presented and the previous works are implemented in different FPGA kit platforms as indicated in the table. Table 1 shows the proposed parallel multiplier using Cyclone IV EP4CGX15BF14C6 has 19.5 % less delay time than the conventional multiplier. It is also less than the reported works in Table 1 that used Virtex-4, Spartan-6 and other FPGA types.

Conclusion

A combination of the truncated and the LSB multiplier circuit are used to design the presented 8-bit parallel multiplier. The LSB multiplier is designed using 2×4 and 4×4 circuit. These circuits are coded Verilog language. Verified to prove the correct results. The proposed designed project includes the LSB and the truncated multiplier circuits is coded, synthesized and gate level simulated on Cyclone IV EP4CGX15BF14C6 FPGA kit to verify the achieved results. The coded circuit required 12.67 ns delay time to run with 107.06 MHZ operating speed. The presented work is proved from the synthesis results that is much more efficient than the classic multiplier by 19.5% in the term of the delay time. It is also having less delay than the reported other works that implemented on different FPGA kit. The achieved results of the proposed parallel multiplier will encourage the designers and industrials to use it in the future electronic circuits and devices.

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