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Design of Prototype Readout Integrated Circuit for Time-of-Arrival and Time-over-Threshold Measurement for Hybrid Pixel X-ray Detectors in 28 nm CMOS

Abstract. *This paper introduces the design and simulation results of a chip prototype dedicated for time-of-arrival (ToA) and time-over-threshold (ToT) measurement of X-ray photons. It consists of 8×4-pixel matrix with 50 µm pitch. Vernier time-to-digital converter with two ring oscillators is implemented in each pixel and aimed ToA resolution is on the order of tens of picoseconds. The chip may work in ToA/ToT mode or single photon counting mode. It is currently in fabrication.*

Streszczenie*. Artykuł przedstawia projekt i wyniki symulacji prototypowego scalonego układu odczytowego do pomiaru czasu uderzenia (ToA) oraz pośredniego pomiaru energii (ToT) fotonów promieniowania X. Układ zawiera matrycę 8×4 pikseli. Piksel ma wymiary 50 µm × 50 µm i zawiera przetwornik czas-cyfra w architekturze Verniera z dwoma oscylatorami pierścieniowymi. Planowana rozdzielczość pomiaru ToA jest rzędu dziesiątek pikosekund. Układ może pracować w trybie ToA/ToT lub w trybie zliczania pojedynczych fotonów. Aktualnie jest w produkcji. (**Projekt prototypowego układu odczytowego do pomiaru czasu uderzenia oraz energii fotonów w hybrydowych pikselowych detektorach promieniowania X w technologii CMOS 28 nm**).*

Keywords: time-of-arrival, time-over-threshold, Vernier time-to-digital converter, hybrid pixel detectors
Słowa kluczowe: czas uderzenia, pośredni pomiar energii, przetwornik czas-cyfra w architekturze Verniera

Introduction

Three-dimensional particle tracking and reconstruction applications in detection systems motivate the development of readout integrated circuits (ROICs) that offer the ability to provide precise timing information about each individual particle. Such functionality proves useful in areas such as antimatter research and electron microscopy [1] and may possibly advance other fields. Two main parameters measured in such systems are: time-of-arrival (ToA) and time-over-threshold (ToT). ToA may be defined as a time difference between the moment when the shutter opens (or closes) and the moment when a particle hits the pixel. In practice, the latter is the moment when the analog front-end (AFE) discriminator output toggles in reaction to particle arrival. ToT is the time during which the discriminator output is in active state, that is when the front-end amplifier (FEA) output is above the discrimination threshold. ToT is a function of an energy of a particle, so it can be used to measure this energy indirectly. One of the most widely used ROICs that offer per-pixel time measurement capability belong to the Timepix family and its predecessors from GOSSIPO family [1-4]. The newest chip, Timepix 4, is designed to provide 200 ps ToA resolution [4].

This paper describes a chip prototype designed in 28 nm CMOS technology, which implements ToA/ToT measurement functionality in 8×4-pixel matrix. This is a continuation of research conducted in microelectronics group in the Department of Measurement and Electronics at the AGH University, which focuses on the development of ROICs for hybrid pixel detectors and applications of such detectors [5-9]. Selected elements of the design and verification environment have already been reported [10-12]. In this paper complete design is summarized and layout is presented. The chip is currently in fabrication.

The design focuses on maximizing ToA measurement resolution while keeping the circuitry suitable for 50 µm × 50 µm pixel. Each pixel includes Vernier time-to-digital converter (TDC) with two ring oscillators. This TDC architecture offers high resolution, even on the order of 5.5 ps, which has been proven in another application, dedicated for digital silicon photomultipliers [13, 14]. In our case, the goal is to achieve the resolution on the order of tens of picoseconds in a ROIC dedicated for X-rays.

Chip Architecture and Layout

Figure 1 illustrates the simplified chip architecture. The system consists of 8×4-pixel matrix and global part. Each pixel includes inverter-based analog front-end with Zimmerman feedback [8]. Signal from the output of a discriminator is then processed in a digital part of the pixel. Alternatively, artificial “discriminator output” test signal may be generated in global part from external Stop and StopToT signals. Which one of these signals is used is determined by per-pixel configuration bit that sets MUX multiplexer select input. Additionally, external Start signal must be generated that sets the start of conversion for ToA. Both Start and discriminator output signals are used by oscillator control module to start or stop both oscillators. Next, oscillator output signals are fed to counters through ToA/SPC, ToT & correction signals module. In this module, additional logic based on pixel configuration is included so that the pixel may operate either in time measurement mode (ToA/ToT), single photon counting (SPC) mode or oscillator calibration mode. Oscillator outputs are also used by coincidence detector module which generates the coincidence signal used for ToA measurement with Vernier method [10, 14]. Coincidence signal also stops the fast oscillator, which ends the ToA conversion, while the slow oscillator is still running and is used for ToT measurement. Additionally, two 1-bit counters are used to generate correction bits used later to compensate for the uncertainty of ToA coarse / ToA fine counter increment signals synchronization.

Oscillator calibration is performed in three steps. Global part includes two 8-bit DACs. One of them sets the common reference for all 32 slow oscillators in the chip while the second one does the same for all 32 fast oscillators. Moreover, each oscillator has its own capacitance bank and 6-bit DAC. Binary-weighted 3-bit capacitance bank loads oscillator nodes and may be used for corner compensation or local mismatch compensation. Local 6-bit DACs are primarily aimed at local mismatch compensation. Granularity of frequency control using local DAC may be adjusted by changing its reference voltage.

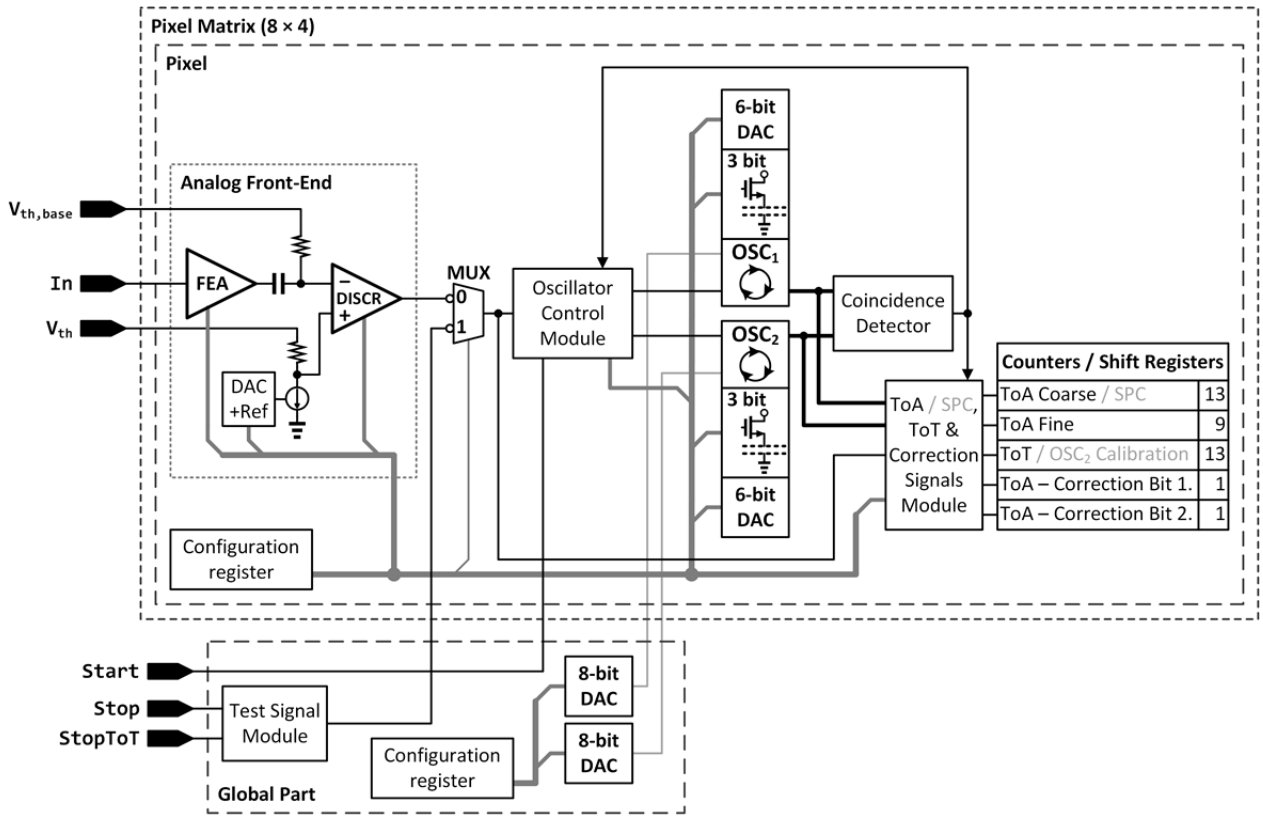

Fig.1. System schematic

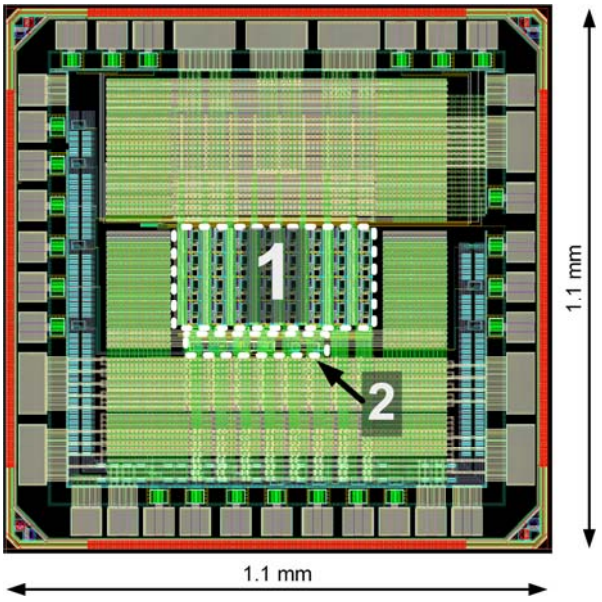

Fig.2. Chip layout: 1 – 8×4-pixel matrix, 2 – global part

Figure 2 presents the layout of the chip. Pixel matrix is in the center and global part is below the matrix. Rest of the die area is filled with decoupling capacitors, and digital I/O buffers with 1.8/0.9 V level converters. Chip area is 1.1 mm × 1.1 mm.

Figure 3 shows the layout of a single 50 µm × 50 µm pixel. Approximately 30% of the pixel is used for analog front-end, while the rest is used for ring oscillators with their calibration blocks as well as digital part and decoupling capacitors. Separate 37-bit counter/data register and 60-bit configuration register are placed at the top and bottom part of the right part of the pixel, respectively. Between these registers there is a pixel logic with coincidence detector, which is also placed as close as possible to both oscillators. Ring oscillators and digital part are surrounded with decoupling capacitors on all sides to separate them from the analog front-end. Additionally, there are three power supply domains, separate for the analog part, ring oscillators with their calibration blocks, and finally the digital part. The last two are also placed in separate deep N-wells to reduce crosstalk and separate bulk supply lines from regular supply lines.

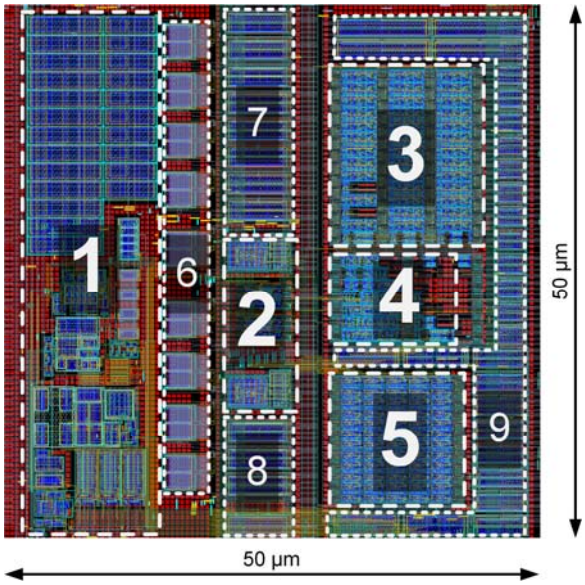

Fig.3. Pixel layout: 1 – analog front-end and references, 2 – oscillators and trimming DACs, 3 – counters/shift registers, 4 – logic and coincidence circuit, 5 – configuration register, 6-9 – decoupling capacitors

Analog Front-End Architecture and Simulation Results

Figure 4 shows the front-end amplifier (FEA) schematic. It is inverter-based amplifier working with the Zimmerman active feedback [8]. Thanks to that architecture the power consumption was decreased, not degrading the amplifiers bandwidth, and FEA area occupation was minimized. The proposed feedback allows for controlling the FEA time response, minimizes detectors leakage current influence and ,unlike other well-known feedback architectures, introduces less noise. To minimize the voltage gain spread the capacitve bank is used built of switchable MOM (Metal-Oxide-Metal) based capacitors each occupying 0.25 um x 2.6 um of area.

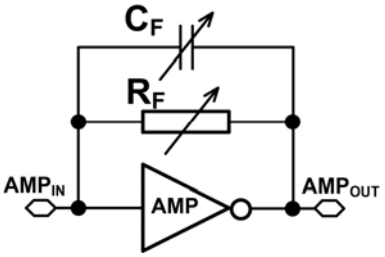

Fig.4. Inverter-based analog front-end

Amplifier output response for different settings of the feedback is presented in figure 5. Linearity characteristics of the FEA is shown in figure 6.

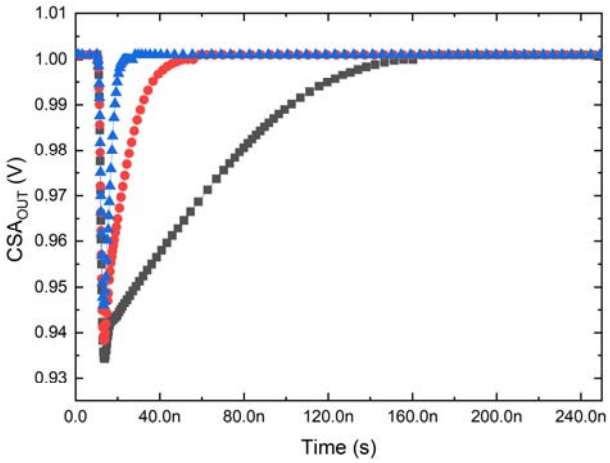

Fig.5. Front-end amplifier's output response for different feedback settings

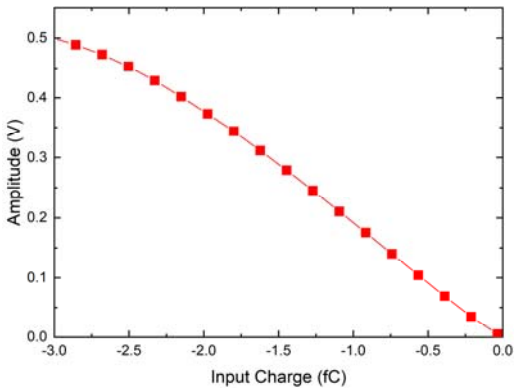

Fig.6. Front-end amplifier's linearity

Ring Oscillator Simulation Results

Oscillator architecture has already been reported in [10]. Capacitance bank has been redesigned since then. Complementary switches have been replaced with single NMOS transistors and metal 1 and 2 have been utilized to create tiny binary-weighted capacitors. As a result, area and power consumption decreased and frequency may be more precisely controlled. Figure 7 presents post-layout characteristics of oscillator output frequency. Global DAC word and capacitance bank settings sweeps were conducted to obtain this plot. It is visible that oscillator frequency can be effectively controlled within 1 GHz to 6 GHz desired range with two mentioned parameters. In the case of capacitance bank, this control comes at the cost of additional power consumption. Additionally, there is still a third method of control available, that is the 6-bit local DAC. Figure 8 shows exemplary post-layout transient simulation of the middle part of the pixel with oscillator frequencies set to 5.1 GHz and 5.8 GHz, respectively.

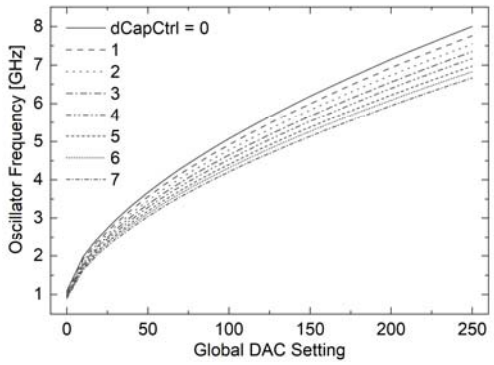

Fig.7. Post-layout ring oscillator simulation result: output frequency as a function of global 8-bit DAC word for all 8 possible settings of capacitance bank (dCapCtrl)

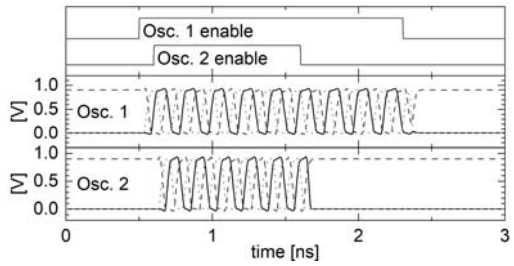

Fig.8. Exemplary transient post-layout simulation of the middle part of the pixel (oscillators with calibration blocks): oscillator enable inputs and three output phases per oscillator are visible

ToA/ToT Measurement Parameters and Simulation Results

Conversion parameters depend on the oscillator output frequencies. Therefore, measurement range, resolution and conversion time may be adjusted to the application requirements. Various compromises are illustrated in Table 1. Available ToA coarse counter and ToT counter length is 13 bits, which limits measurement range. Since fine ToA counter length is 9 bits, it is not going to limit the resolution. When taking into consideration only a digital part of the pixel, measurement precision will be limited by coincidence circuit and oscillator jitter.

To be able to verify digital part of the pixel and obtain transfer characteristics, custom verification environment was prepared using SystemVerilog language [11]. Exemplary transfer characteristics of ToA is shown in Figure 9. Oscillator frequencies were set to 5 GHz and 5.56 GHz to obtain ToA bin width equal to 20 ps. It is visible that desired resolution on the order of tens of picoseconds may be achieved.

Table 1. Exemplary conversion parameters for coarse ToA counter and ToT counter lengths equal to 13 bits

f_{Osc1} [GHz]	f_{Osc2} [GHz]	Fine ToA counter length [bits]	Measurement range [μs]	ToA resolution [ps]	ToA conversion time [ns]	ToT resolution [ps]
1	1.02	6	8.19	19.6	51.0	1000
1	1.11	4	8.19	99.1	10.1	1000
2	2.10	5	4.10	23.8	10.5	500
2	2.50	3	4.10	100.0	2.5	500
3	4.30	2	2.73	100.8	1.1	333
4	4.35	4	2.05	20.1	3.1	250

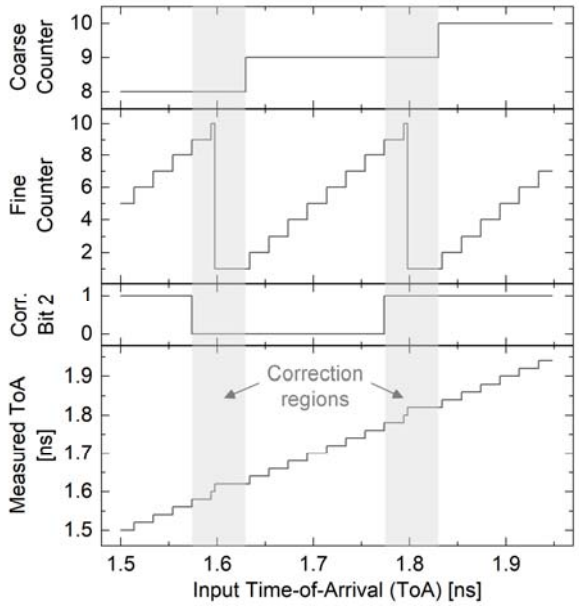

Fig.9. ToA transfer characteristics

Summary

This paper described the design of pixelated chip for ToA/ToT measurement in 28 nm technology. Chip architecture and layout was introduced. Simulation results suggest that ToA resolution on the order of tens of picoseconds is achievable using Vernier TDC with ring oscillators. Chip is currently in fabrication and measurement results are expected in the following months.

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