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Modeling of InAs/Si Electron-Hole Bilayer Tunnel Field Effect Transistor

Streszczenie. *W niniejszej pracy przedstawiamy wyniki modelowania polowego tranzystora tunelowego Si/InAs z biwarstwą elektronowo-dziurową. W tym celu wykorzystaliśmy opracowany numeryczny symulator przyrządów bazujący na samouzgodnionym rozwiązaniu równań Poissona i Schrödingera. Prezentujemy analizę wpływu grubości kanału na charakterystyki prądowo-napięciowe. Pokazujemy, iż wykorzystanie heterostruktury w obszarze kanału przyrządu może dać dodatkową swobodę w konstruowaniu tranzystora tunelowego EHB TFET. (**Modelowanie polowego tranzystora tunelowego InAs/Si z biwarstwą elektronowo-dziurową**)*

Abstract*. In this work, we present the results of modeling of InAs/Si Electron-Hole Bilayer Tunnel Field Effect Transistor. For this purpose, we used a developed numerical device simulator based on a self-consistent solution of Poisson and Schrödinger equations. We present the analysis of the impact of the channel layer thickness on the current-voltage characteristics. We show that using heterostructure in the device channel can give additional freedom in constructing the EHB TFET.*

Słowa kluczowe: modelowanie numeryczne, tunelowanie, TFET, przyrządy półprzewodnikowe.
Keywords: numerical modeling, tunneling, TFET, semiconductor devices.

Introduction

The rapid growth of integrated circuits (IC) performance was possible due to the extreme scaling of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFET). However, new unwanted effects play an important role in deeply scaled devices and degrade their performance [1]. New types of devices are needed to overcome those difficulties. One of the promising candidates is a Tunnel Field Effect Transistor (TFET) [2][3]. Carrier transport in TFETs is based on quantum mechanical effect – interband tunneling [4][5]. Due to this fact it is possible to obtain a subthreshold slope (SS) lower than 60 mV/decade, which is a physical limit for MOSFET [6]. Different types of TFETs were proposed in the literature. In general, classical TFET can be regarded as a gated pin diode with reverse polarization. Electrons tunnel from the source region to the channel region. Gate bias induces an electric field in the channel resulting in proper band bending. It has been pointed out that using low-dimensional carrier gas, one can obtain a very sharp turn-on characteristic of a transistor [7]. Such a device is called Electron-Hole Bilayer Tunnel Field Effect Transistor (EHB TFET). There are works presenting a study of EHB TFET for different channel materials [8-12]. Whereas there are not many works regarding the modeling of heterostructure TFETs. In this work, we modeled the electrical characteristics of heterostructure EHB TFET and studied the effect of InAs/Si channel layer thickness on the current-voltage characteristics. We show that using heterostructure in the device's channel can result in a higher drain current.

Theory

In Figure 1, we show a schematic picture of the considered device. We consider a transport between 2D electron gas (2DEG) and 2D hole gas (2DHG) in the x-direction. We assume that 2DEG and 2DHG are in thermal equilibrium with drain and source regions, respectively. The drain-source voltage is related to the positions of quasi-Fermi levels of 2D gases. In order to obtain electrostatics in the structure, we solved the Poisson equation and Schrödinger equations for electrons and holes in a self-consistent manner.

$$\nabla(\varepsilon\nabla\varphi) = -q(p - n - N_A) \tag{1}$$

$$\left(\mp\frac{\hbar^2}{2}\nabla\frac{1}{m_{c/v}}\nabla + V_{c/v}\right)\Psi_{c/v} = E\Psi_{c/v} \tag{2}$$

where φ is the potential within the structure, ε is the electrical permittivity, p and n are hole and electron concentrations, N_A is the acceptor concentration, m_c and m_v are effective masses of electrons and holes, V is a band edge energy of conduction and valence bands, E is total energy, Ψ is a wavefunction.

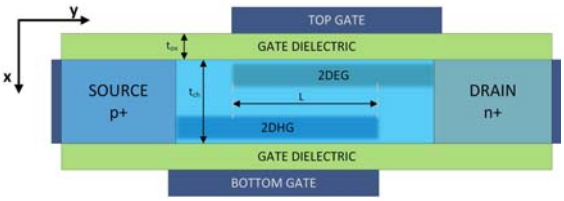

Fig.1. Schematic picture of EHB TFET

Depending on the type of material, direct or indirect band structure, a proper model describing current density needs to be used [13][14]. Direct interband tunneling current is calculated according to

$$J_{dir} = \frac{4\pi q}{\hbar}\sum_{\mathrm{n}}\sum_k |M|^2\, JDOS_{2D}\,[f_c - f_v] \tag{3}$$

where we sum contributions to the current from different energy levels from conduction and valence band. Coupling coefficient $|M|^2$ of the 2D-2D tunneling system is calculated based on the Bardeen's transfer Hamiltonian approach, assuming conservation of the total energy and parallel momentum in the system. Details of the model used in this work are presented in work [11].

Results and discussion

In our work, we used a developed numerical device simulator based on a self-consistent solution of Poisson and Schrödinger equations in 1D. The physics-based models were implemented in a computer program coded in C. LAPACK and BLAS numerical libraries were used to solve linear equations and eigenvalue problems. We used the developed simulator to calculate I-V characteristics of EHB

TFETs of different channel materials [15]. Obtained results are comparable to simulation results presented by other authors using similar models.

We performed simulations for Si/InAs EHB TFET using the following parameters: doping level of the channel $N_a=10^{15}$ cm^{-3}, channel length L = 50 nm, gate oxide thickness t_{ox}=3 nm, gate oxide relative electrical permittivity ε_r=22. We varied the channel thickness t_{ch}. We adjusted the work function of bottom-gate Φ_{BG} in a way that 2DHG is induced at bottom gate-source voltage V_{BG}=0, and we varied only top gate-source voltage V_{TG}. Material parameters used in the simulation are presented in Table 1.

Table 1. Simulation parameters of materials

	Si	InAs
E_G	1.12 eV @ Δ	0.354 eV @ Γ
m_{hh}	$0.49m_0$	$0.41m_0$
m_{hl}	$0.16m_0$	$0.026m_0$
m_Γ	-	$0.023m_0$
m_t	$0.19m_0$ @ Δ	-
m_l	$0.916m_0$ @ Δ	-

In one of our previous work [15] we studied the current-voltage characteristics of EHB TFET for Si, InAs and Ge channel material. We modeled and analyzed the I-V characteristic of different devices. Simulation results for Si and InAs TFETs show that Si EHB TFET has a much lower current than InAs EHB TFET due to the indirect bandgap. InAs device offers much higher ON-current and very steep current-voltage characteristics due to direct bandgap. In the case of Si/InAs heterostructure band to band tunneling is mainly direct tunneling process, as confirmed by quantum mechanical simulations presented in work [16]. Due to this fact, in our considerations we used formula (3) to calculate the current.

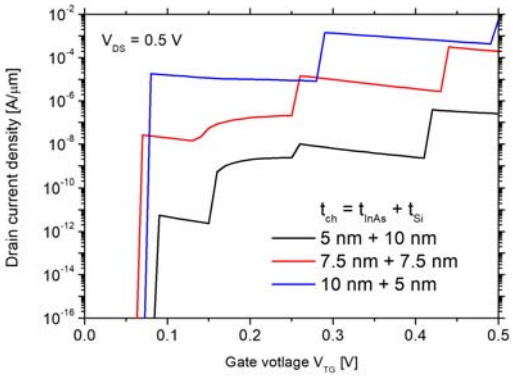

Fig.2. Current-voltage characteristics of EHB TFET for t_{ch} = 15 nm, V_{DS} = 0.5 V and different InAs/Si layer thickness ratio (Φ_{TG}=4.7 eV Φ_{BG} = 5.6 eV).

In Figure 2, we show the current-voltage characteristics of InAs/Si EHB TFET for t_{ch}=15 nm, V_{DS}=0.5 V. Depending on the thickness of InAs and Si layers, we observe the different shapes of I-V curve. Different current steps are related to the alignment of the electron and hole sub-band energy levels. Therefore, the tunneling process is possible and contributes to the total current. Within the investigated geometric parameters, we observed that reducing Si thickness results in higher current. In Figure 3, we compare I-V characteristics for different t_{ch} values and the same InAs/Si layer thickness ratio. Channel layer thickness of 10 nm results with very sharp turn-on characteristic and shift in voltage at which first electron and hole sub-band energy levels align. It can be adjusted using a metal gate with different work function.

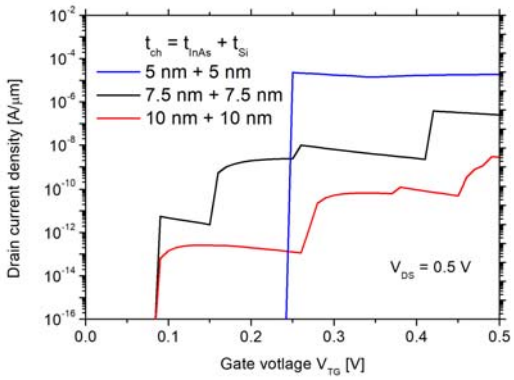

Fig.3. Current-voltage characteristics of EHB TFET for different t_{ch}, V_{DS} = 0.5 V and the same InAs/Si layer thickness ratio (Φ_{TG}=4.7 eV Φ_{BG} = 5.6 eV).

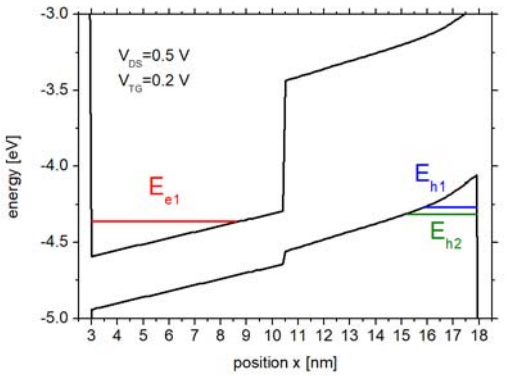

Fig.4. InAs/Si EHB TFET energy band diagram and energy levels for V_{DS} = 0.5 V, V_{TG} = 0.2 V and t_{ch} = 15 nm (InAs/Si = 7.5 nm/7.5 nm).

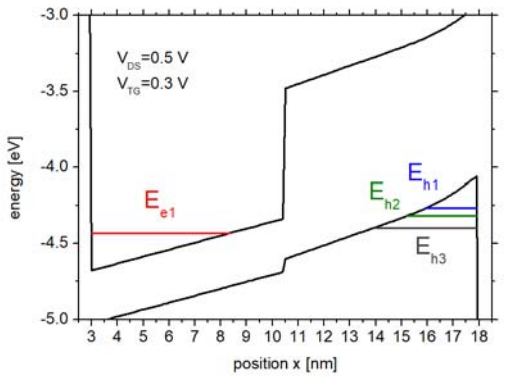

Fig.5. InAs/Si EHB TFET energy band diagram and energy levels for V_{DS} = 0.5 V, V_{TG} = 0.3 V and t_{ch} = 15 nm (InAs/Si = 7.5 nm/7.5 nm).

In Figures 4-5 we present the energy band diagram in a cross-section of the device channel along x-axis for t_{ch} = 15 nm (InAs/Si = 7.5 nm/7.5 nm), V_{DS} = 0.5 V and different V_{TG} values. Quantum confinement results in discrete energy levels. For V_{TG} = 0.2 V, we observe that tunneling is possible between the first electron energy level 2DEG and two energy levels in 2DHG (first energy levels of heavy and light holes). For V_{TG} = 0.3 V, there is an additional hole energy level that allows for tunneling and contributes to the total tunneling current. It results in a current rise above 0.2 V visible in Figure 2.

In Figure 6, we show energy band diagram for t_{ch} = 10 nm (InAs/Si = 5 nm/5 nm), V_{DS} = 0.5 V and V_{TG} = 0.3 V.

Band to band tunneling is possible only between first electron and hole sub-band energy levels. However, we obtain a higher device current (see Figure 3) due to a shorter tunneling path at the same gate voltage bias.

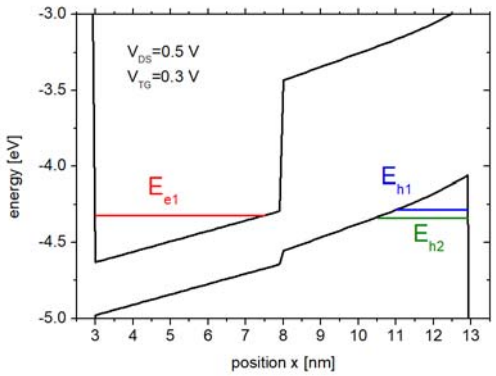

Fig.6. InAs/Si EHB TFET energy band diagram and energy levels for V_{DS} = 0.5 V, V_{TG} = 0.3 V and t_{ch} = 10 nm (InAs/Si = 5 nm/5 nm).

Conclusions

This paper presents the quantum mechanical numerical modeling of InAs/Si Electron-Hole Bilayer Tunnel Field-Effect Transistor. We show that tunneling between discrete energy levels of 2D hole and 2D electron gases can result in a very sharp turn-on characteristic. We analyze the impact of the channel layer thickness on the current-voltage characteristics. We explain the shape of the I-V curves based on energy band diagrams in a cross-section of the device channel and the position of sub-band energy levels. Using heterostructure in the device channel gives additional freedom in constructing the EHB TFET and can result in shorter tunneling path for electrons, particularly when proper band alignment can be obtained (like in the case of Si and InAs).

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