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Modeling of 81-Level Inverter Based on a Novel Control Technique

Abstract: *Multilevel cascaded inverters using the similar DC source values are applied with limited total harmonic distortion (THD). This paper presents multilevel inverter with unequal DC voltage source values and less power switching devices to get different output voltages with different levels. Single-phase four H-bridge inverter cells with DC voltage values of Vdc, 3Vdc, 9Vdc and 27Vdc are adopted and modelled by MATLAB program with resistive and inductive loads. A new control technique, modified absolute sinusoidal PWM (MASPWM), is designed and employed to drive the switching devices of the multilevel inverter to catch output inverter voltage with levels from 3-level to 81-level. That means, it has the ability to get voltage with any required level. Simulation results indicate that the THD magnitudes of the AC current and voltage are changed form 22% and 13.3% to 1.55% and 0.79% for 5-level to 81-level, respectively.*

Streszczenie. *Wielopoziomowe falowniki kaskadowe wykorzystujące podobne wartości źródła prądu stałego są stosowane z ograniczonym całkowitym zniekształceniem harmonicznym (THD). W artykule przedstawiono wielopoziomowy falownik o nierównych wartościach źródła napięcia stałego i mniejszej liczbie urządzeń przełączających moc w celu uzyskania różnych napięć wyjściowych o różnych poziomach. Jednofazowe cztery ogniwa inwertorowe z mostkiem H o wartościach napięcia stałego Vdc, 3Vdc, 9Vdc i 27Vdc są przyjęte i modelowane przez program MATLAB z obciążeniami rezystancyjnymi i indukcyjnymi. Nowa technika sterowania, zmodyfikowana bezwzględna sinusoidalna PWM (MASPWM), została zaprojektowana i zastosowana do sterowania urządzeniami przełączającymi wielopoziomowego falownika w celu wychwycenia wyjściowego napięcia falownika o poziomach od 3-poziomowego do 81-poziomowego. Oznacza to, że ma możliwość uzyskania napięcia na dowolnym wymaganym poziomie. Wyniki symulacji wskazują, że wartości THD prądu i napięcia AC zmieniają się odpowiednio z 22% i 13,3% do 1,55% i 0,79% dla poziomu 5-poziomowego do 81-poziomowego.* (***Modelowanie 81-poziomowego falownika w oparciu o nowatorską technikę sterowania***)

Keywords: multilevel cascaded H-bridge inverter, MASPWM, 81-level, unequal DC voltage sources.
Słowa kluczowe: Przrksztaltnik wielopoziomowy, MASPWM, przekształtnik 81-poziomowy

Introduction

The power inverters contain a collection of switches that converting DC input voltages to AC voltages. Since the output is not a pure sine wave; the output waveforms of the inverter may be categorized as a square-wave output inverter, quasi-square-wave output inverter, commercial two-level inverter and multilevel-wave inverter as illustrated in Fig.1 [1]. A sinusoidal voltage could be generated by using a silicon carbide (SiC) switches inverter [2-4] or by using a multilevel inverter with high number of levels [5]. The SiC switches are more expansive than silicon switches. In addition, that, this switch type requires high reliability controller due to high and fast switching frequency in order to get the required output voltage compared with the conventional types. Multilevel inverters have the ability to produce higher voltage quality, less electromagnetic interference, lower switching losses and stress, and better performance [6-8]. The voltage quality here means that the multilevel inverter produces higher voltage and less total harmonics distortion (THD) compared with conventional type. The multilevel inverters play an important role in many industrial power applications like grid connection applications [9], fuel cell and photovoltaic applications [10, 11], electric vehicle systems [12], and low power load applications [13]. The multilevel inverter circuit is used in many industrial power applications like roll mills, paper industry, electric-vehicles, drive machines, motoring and regenerative braking, flexible AC transmission systems, power quality control, etc. The modelling, simulations, and implementation of a multilevel inverter that converts a DC voltage to an AC voltage was presented [14]. The main configurations of multilevel converter topology are flying capacitors multilevel inverter, cascaded H-bridge multilevel inverter, and diode clamped multilevel inverter [10, 14-16]. In [17], the optimum adjacent level control scheme was used to present the extended cascaded multilevel converter, with half-bridge and even without half-bridge connections, the main units and their cascaded interconnections were examined. In 2021 [18], the suitability of the inverter for industrial applications was discussed using various type of multilevel inverter to deal with challenges in producing more output voltage levels with switching number devices and techniques of modulations. The use of a switched capacitor component in a new multilevel inverter architecture was presented to generate a higher levels number at the output with fewer components. With two diodes, two capacitors, two DC sources, and ten switches, the basic presented construction generates a 17-level output voltage [19]. In [20], 9-level inverter was developed and simulated with a single DC source coming from a solar photovoltaic (PV) module. The control scheme provides more precise results and lowers power loss while maintaining high power quality. The suggested methodology removes specified harmonics by cutting out the fundamental element at predefined switching angles, analysis of the data obtained for the inverter. In 2018 [21], Single and three phases 27-level cascaded inverter with input voltages equal to 1Vdc, 3Vdc and 9Vdc and modified absolute sinusoidal pulse width modulation (MASPWM) strategy with inductive load was simulated by MATLAB. The THD values of the load current and voltage for single-phase-circuit were 0.238% and 1.165%, while were 0.67% and 0.0857% for three-phase circuit, respectively. The suggested circuit with its controller proved its effectiveness for reducing distortion in the load voltages and currents. In 2020 [22], the same circuit with same controller used to control induction motor without sensors. Speed and torque of the induction motor were sensorless controlled at different operation conditions. The system gave good response and quality. Also, an optimum number of switches was considered many topologies of the cascaded multilevel inverter (MLI), an enhanced number of switches, modified circuits of the gate driver, and a maximum of 351 levels of voltage was presented. For producing a required number of the voltage levels, a selected values of DC supplies were offered [23]. Three phase cascaded inverter was suggested to have a discontinuous PWM in order to scale down the switching losses so that the switches lifetime is enhanced. Additionally, the MLI have a rotation scheme design in order to get even power distribution in the switches [24]. A mix between a cascaded H-Bridge module and switched-capacitor component was proposed in [25], a maximum level of the output voltage is produced by connected the capacitor component -which is acts like a DC source- in series with the DC source Voltage. A novel design for forming an insulated single-phase MLI for on-grid connection was designed based a standard three-phase inverter and transformer [26], it is presents that the control scheme, which is focused on the mode of operation of an interconnected transformer, demonstrates how the low impedance of magnetic legs may be used to develop a cascaded layout by combining multiple inverters to every terminal of both leg coils. In [27], a good start with reduced switch count- symmetric multilevel inverter setup was introduced. The suggested topology uses a new switched-dc-source separated DC source (SDCS) subsystem to regulate the DC voltage of the four DC input supplies via three switching devices. A significant number of the system output voltage levels can be produced with a decreased number of required switching devices by connecting the suggested SDCS in series in a novel circuit arrangement.

As a continuance of the previous study to get a complete understanding of multilevel inverter, an 81-level inverter with less power switching device and low distortion has been employed in this paper. This paper used a MASPWM controller technique proposed by [21-22] as a new control strategy of an 81-level inverter. The novelty of the projected system is to get high capacity power with low THD and produce different levels from 5-level to 81-level. The contribution of the proposed study is to raise the electrical power efficiency.

Circuit topology

For conventional type and to produce 81-level of output voltage, forty cascade H-bridge voltage source inverter are connected in a series with forty equal DC voltage source where 160 power electronic switching devices are required [28-31] as shown in Fig.2. In this study, four H-bridge inverters with an input voltage equal to Vdc, 3Vdc, 9Vdc and 27Vdc are designed and implemented using MATLAB program as depicted in Fig.3. The summation of input voltages is equal to 40Vdc (1:3:9:27) and the 81-level output voltage is consisting of 40-level in the positive half cycle and 40-level in the negative half cycle beside the zero-level. The output voltages of each H-bridge unit (VHB1, VHB2, VHB3 and VHB4) will be surmised to get the total output voltage of the inverter.

Number of switches and SDCSs in the conventional MLI circuit are:

(1) No. of switches = 2(L–1)

(2) No. of SDCS= (L – 1)/2

While in the recommended power circuit, number of switches and SDCSs are selected as:

(3) No. of switches = (L–1)/5

(4) No. of SDCS = (L – 1)/20

This topology needs 16-switches and 4 SDCSs to produce 81-level. Therefore, number of switches and SDCSs is minimized by 90%, respectively. The factor (L) represents the output voltage level.

MASPWM controller strategy

Different PWM techniques have been utilized with multilevel inverters to minimize THD. In this study, MASPWM controller strategy used by [21-22] has been redesigned to match the proposed power circuit and gotten 81-level voltage as explained in Fig.4. The first part of the MASPWM controller is generating reference sine signal with absolute value that represent the wanted output voltage level. Then converting this signal to stairs signal and the difference between them produces the MASPWM signal.

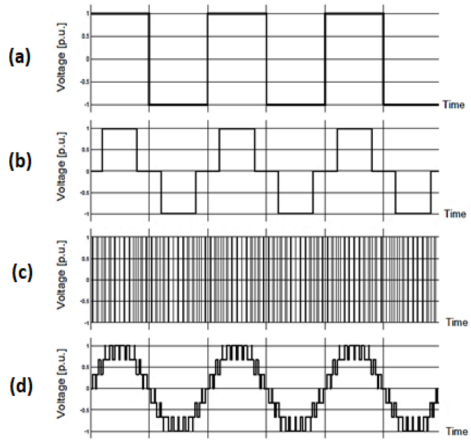


Fig. 1 Classic inverter output waveforms of (a) Square, (b) Quasi-square, (c) Commercial two-level, and (d) Multilevel waves.

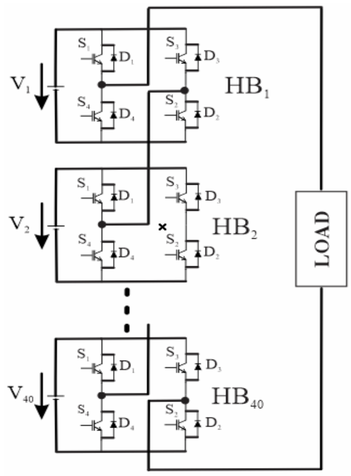


Fig. 2 Commercial 81-level inverter

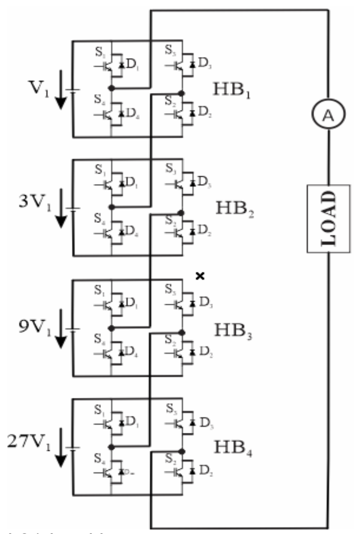


Fig. 3 Proposed 81-level inverter

The difference between the stairs signal and absolute sinusoidal signal represents the MASPWM signal as shown in Fig. 4. This signal is compared with one triangle signal and produce one PWM pulse. The IGBTs pulses of MLI is regenerated and dispersed using MATLAB s-function which is also used to select the patterns of the IGBTs switching state operation. Additionally, the layout of the control circuit is arranged to generate various output inverter levels according to the DC supplies organization, Fig.5. Consequently, and due to unequal input DC input voltages, 81-levels of Vdc are presented in the MLI output.

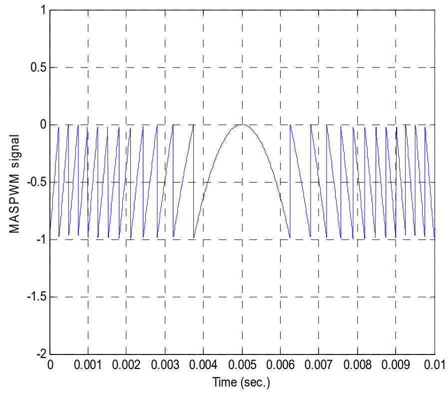


Fig. 4 MASPWM signal.

Simulation results

The designed MLI is improved using unequal input DC input source to get different output levels. The Vdc and switching frequency values are chosen as 30 V and 3 kHz. Modelling results of the output current and voltage along with its FFT of the lowest level (5-level), 41-level, and highest level (81-level) with resistive and inductive (0.8 lag) loads are explained in Fig.6, Fig.7 and Fig.8, respectively. The THD value of the 81-level output voltage and current is 1.558% and 0.799% for inductive load. On the other hand, the THD for 41-level and 5-level output voltage and current is 2.8433% and 1.4714%, and 22.2122% and 13.3833%, respectively. In order to get the complete understanding of the MASPWM with different levels, THD of the output MLI current and voltage at a number of levels is illustrated in Fig. 9. The waveform presents that the THD values are implied in the standards based on MASPWM algorithm. The dynamic and steady-state output voltage and current waveform with levels (5-level to 81-level) is explained in the Fig. 10. This figure showed that the system is efficient to work at any required level voltage with good THD.

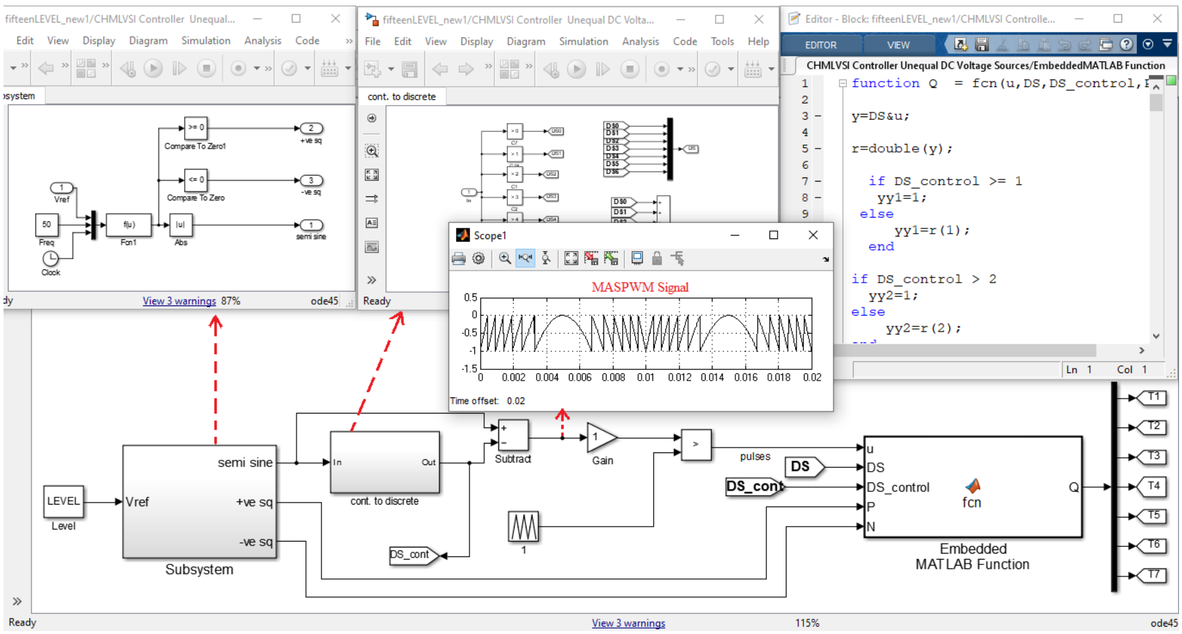
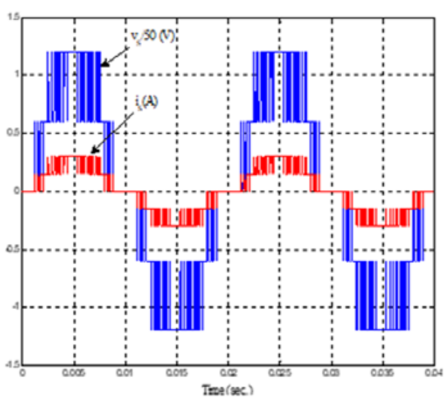
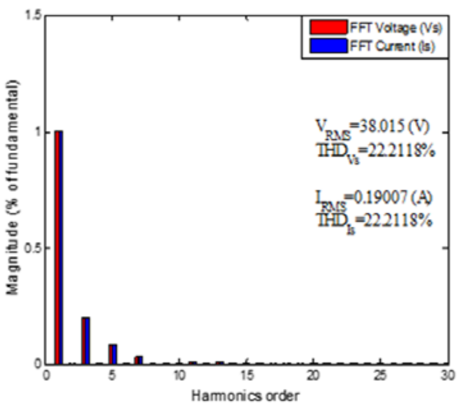


Fig.5 Suggested controller circuit

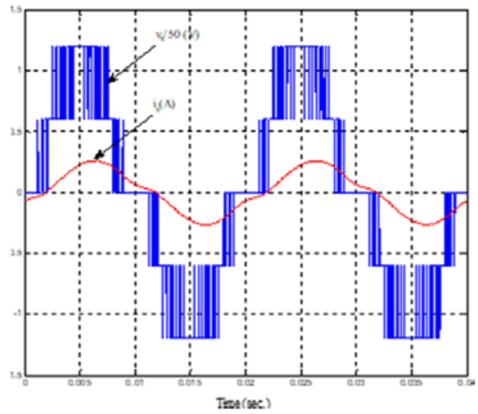
a)



b)



c)



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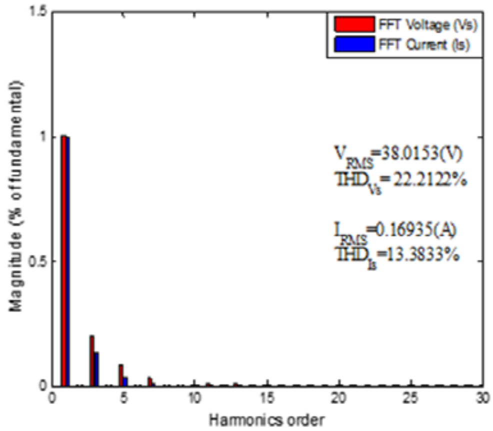
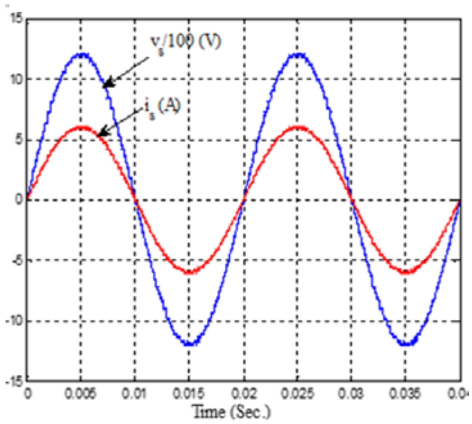


Fig. 6 Simulation results of 5-level (a) output voltage and current and it's (b) FFT for R-Load, and (c) output voltage and current and it's (d) FFT for RL-Load

a)



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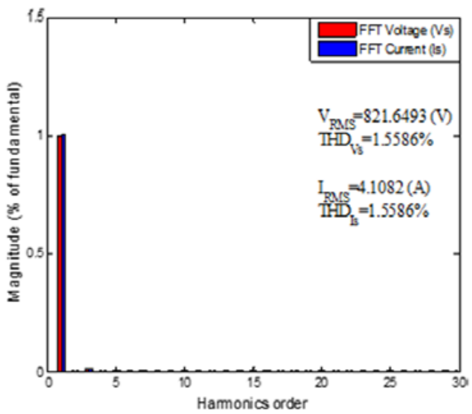

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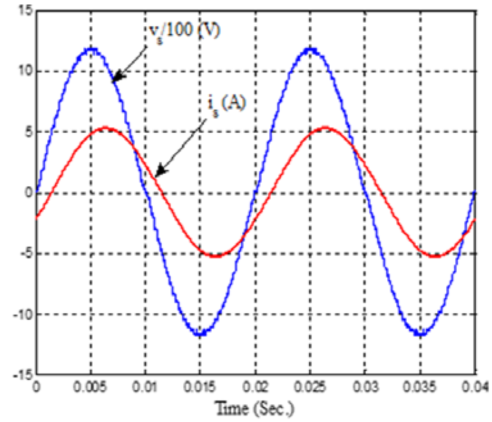


d)

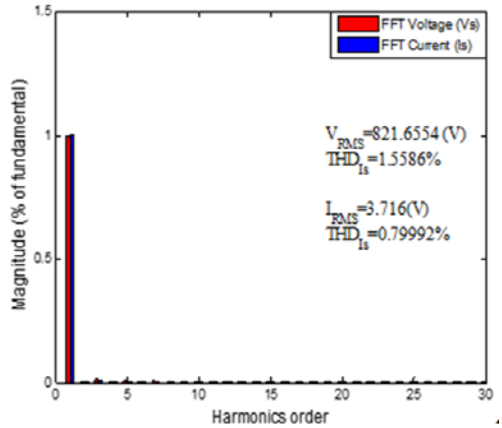
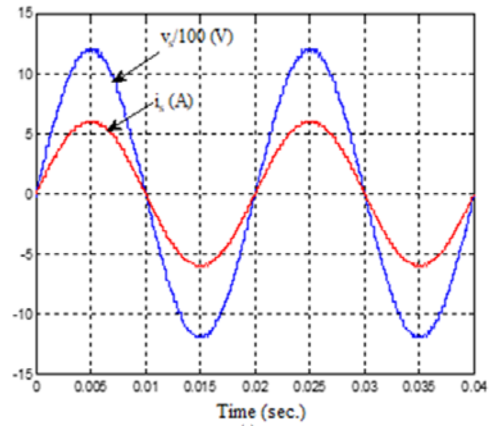
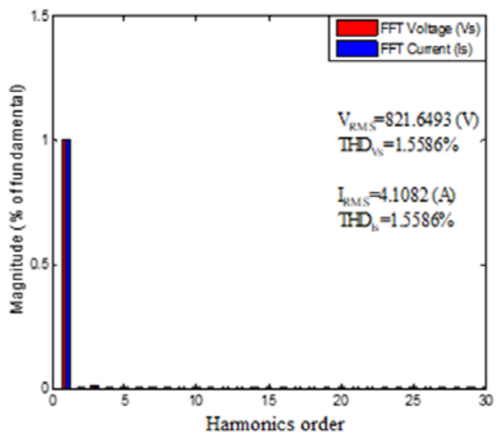


Fig. 7 Modelling results of 41-level (a) output current and voltage and it's (b) FFT for R-Load, and (c) output voltage and current and it's (d) FFT for RL-Load

a)



b)



c)

d)

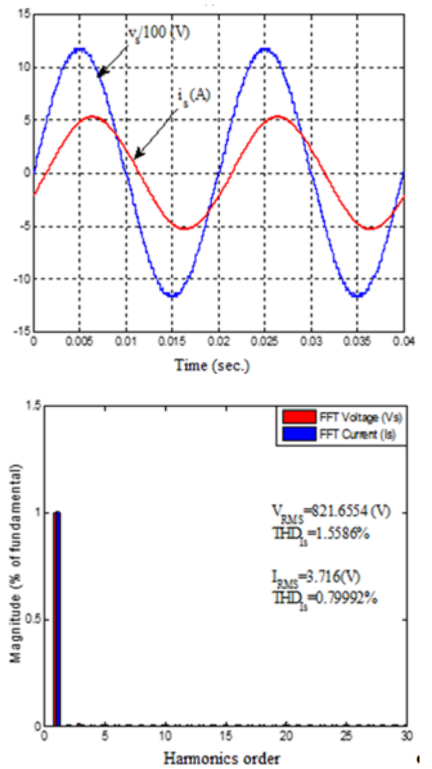


Fig. 8 Modelling results of 81-level (a) output current and voltage and it's (b) FFT for R-Load, and (c) output voltage and current and it's (d) FFT for RL-Load

a)

b)

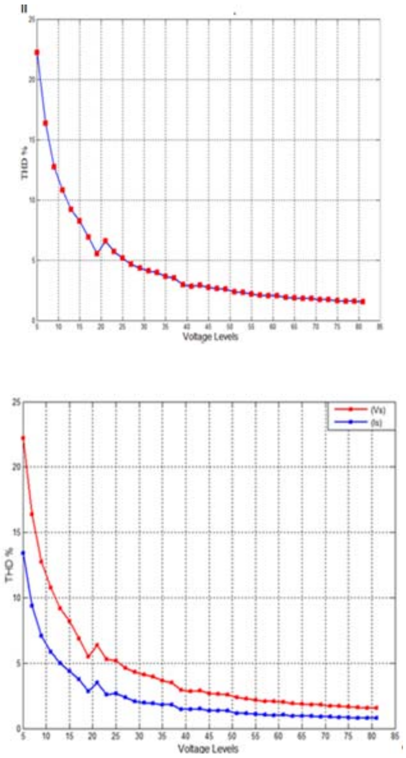


Fig.9 THD of the output current and voltage (a) resistive and (b) inductive load

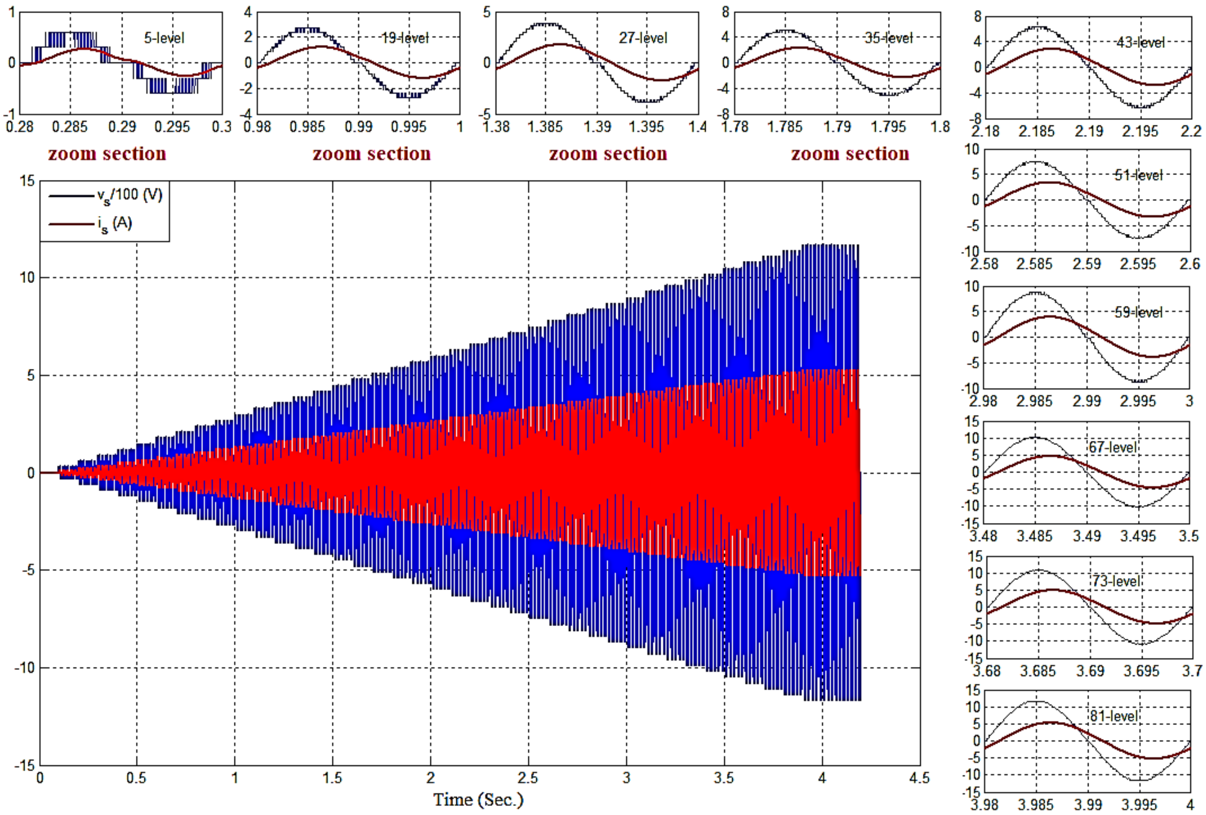


Fig.10 Output MLI current and voltage waveform.

Conclusion

The study aims to illustrate a single-phase MLI with resistive and inductive load using a MASPWM control technique that suggested by [21-22]. Four H-bridge inverter cells are used with DC voltage source of Vdc, 3Vdc, 9Vdc and 27Vdc in order to generate eighty-one level output voltage unlike the conventional type. Furthermore, this paper presents different levels of THD with resistive and inductive loads.smli From simulation results, the effective harmonic orders of the output voltage and current can be removed and THD values are within limits. Moreover, adequate power quality is resulted for various voltage levels either in steady state or in transient conditions. The total cost and size of the proposed MLI circuit are less than conventional types because of number of switching devices and SDCSs are decreased by 90%. Interestingly, in industrial applications, it is appropriate to use this kind of MLI with the suggested MASPWM strategy especially when regulating speed drive is needed.

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