SilTerra Malaysia Sdn. Bhd (1), Universiti Teknikal Malaysia Melaka (2), Universiti Malaysia Sarawak (3) ORCID: 1.0000-0002-9172-7605; 2.0000-0002-9404-5562

doi:10.15199/48.2022.03.14

Experimental Quantification of Electrostatic Damage (ESD) in Binary Reticle with Feature of Nanometre Scale Gaps

Abstract. A Binary reticle for lithography circuit patterning is extremerly senstive to electrostatic field. Damaged is seen on its feature after a breakdown voltage occurred between the metal lines. The experimental quantification of ESD for Binary reticle is performed by direct discharge to the feature of Critical Dimension (CD) of 80 nm to 160 nm. Its breakdown voltage correlated to CD but lower than international standard recommendations and observed Electric Field-Induced Migration (EFM) damaged at CD of < 110 nm but ESD for CD > 110 nm to 160 nm.

Streszczenie. Siatka binarna do wzorcowania obwodów litograficznych jest niezwykle wrażliwa na pole elektrostatyczne. Uszkodzenie jest widoczne na jego cechach po wystąpieniu napięcia przebicia między metalowymi liniami. Eksperymentalne oznaczenie ilościowe ESD dla siatki binarnej jest wykonywane przez bezpośrednie wyładowanie do cechy wymiaru krytycznego (CD) od 80 nm do 160 nm. Jego napięcie przebicia było skorelowane z CD, ale niższe niż zalecenia międzynarodowych standardów i zaobserwowano migrację indukowaną polem elektrycznym (EFM) uszkodzoną przy CD < 110 nm, ale ESD dla CD > 110 nm do 160 nm (Eksperymentalna ocena ilościowa uszkodzeń elektrostatycznych (ESD) w siatce binarnej z cechą przerw w skali nanometrycznej)

Keywords: ESD, EFM, Paschen law, and Townsend-Fowler Nordheim field emission. **Słowa kluczowe**: wyładowania elektrostatyczne ESD, siatka ekranująca

Introduction

A reticle is like a template or stencil which is used in a photolithography process to project a desired pattern onto the wafer surface [1], [2]. Typically fifty reticles will be used to complete a Complementary Metal Oxide Semiconductor (CMOS) device. Each reticle is named according to layer of process steps of device fabrication such as poly, metal, via, contact, and trench [3]. A Binary reticle is constructed of a high-purity quartz substrate with thickness approximately 6.35 mm that has a nanometre layer (~100 nm) of chromium (Cr) on the surface which has been etched into patterns called features [4]. It is Extremely Electrostatic Sensitive (EES) device and can be damaged when it is exposed to a low electric field [5], [6]. The Binary reticle feature consists of many individual single lines of Cr on top of quartz substrate. The features became isolated from ground because of the quartz substrate which an insulator [7]. Whenever reticle exposed to a nearby electrostatic charged object, the Cr lines will be polarized to multi potential voltage levels by the electric field. The Cr line which is nearest to the charged object will be induced with higher potential than the farthest Cr line and thus create potential difference between the Cr lines. A breakdown voltage will occurred if the potential difference between the Cr lines exceeds its threshold voltage [8], [9]. There are two mechanism of a breakdown voltage which is high voltage discharge or Paschen spark and low voltage discharge or Townsend-Fowler Nordheim field emission.

Paschen law and Townsend field emission (corona discharged) are theories that define electrical breakdown voltage between two parallel conductors. Paschen law defines the breakdown voltage as a simple function of the gas pressure and the electrode spacing of a natural gaseous matter under a constant electric field [10], [11]. The formula for Paschen breakdown voltage is,

(1)
$$\dots V_b = \frac{Bpd}{\ln[Apd/\ln(1+1/\gamma)]}$$

where: p - pressure, d - gap spacing, and γ - secondary ionization coefficient. The A and B are the coefficients that are associated with the ionization coefficient α , which is in a molecular gaseous form, and E is the electric field [10].

(2)
$$\alpha = Ape^{\left(\frac{-Bp}{E}\right)}$$

In short, the breakdown voltage Vb is exclusively dependent on the product of pressure (p) and electrode gap distance (d) [11]. The breakdown voltage at smaller gap spacing is influenced by secondary ionization instead of pressure at a constant electrostatic field [11]. Secondary ionization processes by which secondary electrons are produced sustain a discharge after being established due to ionization by collision and photo-ionization [12]. The main factors that promote secondary ionization are electrostatic field strength and electrode metal work function. In summary, at smaller gap spacing breakdown voltage, Townsend field emission (secondary ionization) influences more than the Paschen law. The Townsend field emission is determined by electrostatic field strength and electrode metal work function. The cathode requires a sufficient electrostatic field to ionize the air, and gap space between electrodes long enough for an avalanche to build up. However, as the gap reduces, the excitation energy of the cathode influences more on breakdown voltage than electrostatic field strength. The excitation energy of the electrode is directly proportional to the work function of a metal [10]-[12],

(3)
$$E = \frac{\pi \epsilon_0 \Phi^2}{e^3}$$

where: E is the electric field, e is electron charge, ϵ_0 permittivity of the vacuum and ϕ - work function of metal (nickel electrodes, ϕ = 4.6 eV and aluminium, ϕ = 3 eV).

The aftermath of Paschen spark will be observed as a burnt mark or mouse bite defect due to high voltage discharged which released high energy [13]. However the damage mechanism of Townsend-Fowler Nordheim aftermath is EFM where a portion of Cr line diffused to the adjacent Cr line as shown in Figure 1 after multiple low discharged [6], [14].

In other words, a Binary reticle can absorb some electrostatic stress without suffering an ESD event because a certain voltage threshold must be reached before a spark can take place. At a feature spacing of 1000 nm this has been shown to be around 150 V, so a level of electric field exposure that does not induce this voltage between the reticle features will not cause ESD [15]. However, the characteristics of reticle damage change as feature spacing is reduced. It is expected EFM damage to the reticle with features of nanometre scale gaps since the breakdown voltage conform to field emission theory.

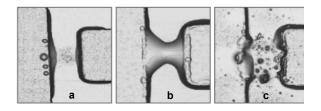


Fig.1. The transformation of reticle feature from the effect of EFM. A metal continuous diffuse (a) to adjacent metal until complete bridging (b) and end up vaporised (c) [14]

Minimize the electrostatic charges on reticle below the reticle Electrostatic Discharge (ESD) threshold voltage are the measures taken by semiconductor manufacturing to prevent the reticle from damaged. International Technology Roadmap for Semiconductors (ITRS) and Semiconductor Equipment Materials International (SEMI) has established a recommendation of maximum allowable on facilities and reticle surfaces [5], [16]–[18]. The ITRS recommendation of maximum allowable electrostatic field on wafer and photomask surfaces is shown in Table 1.

Table 1. The static charge recommendation of ITRS [17]

Technology node	180 nm	130 nm	100 nm	90 nm	80 nm
Maximum allowable electrostatic field on wafer and photomask surfaces	200 V/cm	150 V/cm	125 V/cm	100 V/cm	90 V/cm

Table 1 was established based on tests conducted on a Binary reticle with 1,500 nm gap between metal lines. The result of the characterization has been extrapolated and defined for smaller technology nodes [19]. Using 1,000 to 1,500 nm technology node ESD threshold voltage characterization and extrapolated it, lead to inaccurate determination of ESD threshold voltage for smaller technology node due to beyond the range set of data [20]. In this research, the experimental quantification is carried out on actual Binary reticle of < 250 nm which is 4 to 6 times smaller than ITRS. The result can be used to validate the accuracy of ITRS and SEMI recommendation of ESD threshold voltage for Binary reticle as well as to quantify the ESD defects [14], [15].

Materials and Methods

The Binary reticle test plate design is a single line feature as shown in Figure 2. The design is similar to other researchers design [14], [15]. It has 2 main component which are cathode (body and spur) and anode (border). The cathode will be the pad which direct current applies to it during electrostatic direct discharge test.

The body and chrome border size are fixed at 25,000 nm (c, d, and e) and the design followed the previous researcher's design [11]. The body and chrome borders size are wide enough as a test pad for probing. The spur width (b) is fixed at 250 nm to ensure the same corona effect [7]. The gap distance (a) between the spur and chrome border varies according to technology nodes of 80, 90, 110, 130 and 160 nm.

The Binary reticle test plate was quantified using electrostatic direct discharge tester [13]–[15]. The tester setup is shown in Figure 3. A source/measure meter, HP

4145B semiconductor parameter analyser which can supply voltage and measure current simultaneously is connected to the test probes. One probe is placed on the feature's body and another probe on the border. The probes were carefully placed on the feature using a micro-positioner jig to ensure good contact and avoid damage to the surface. The cables were clamped using TEK CT-6 current probes

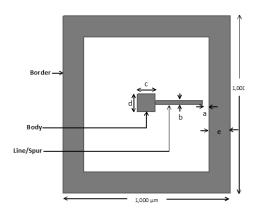


Fig.2. Single line feature design reticle test plate

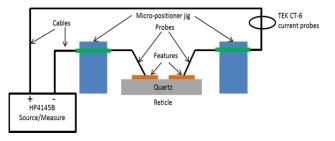


Fig.3. The schematic representation of electrostatic direct discharge test

A DC voltage will be applied directly to the body whereas the border will be connected to ground. The DC voltage was ramped from 0 - 100 Volts at 0.5 Volts step increment. The current will be measured simultaneously during the ramp up voltage. A visual inspection was carried out before and after the electrostatic direct discharge test. The purpose of the visual inspection was to verify for any defects at the spur and border [14], [15]. A microscope at 100x magnification is used to for the visual inspection.

Results and discussion

The current and voltage are recorded during the direct discharge test at each feature. The current-voltage or IV curve for 80, 90, 110, 130 and 160 nm is shown in Figure 4.

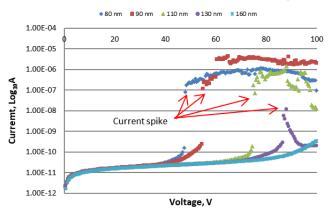


Fig.4. The IV curve of direct discharge test on Binary reticle feature with gap distance of 80, 90, 110, 130 and 160 nm $\,$

The first current spike was observed on feature of 80 nm gap width when the DC voltage reached 48.5 V. Similar observations for other feature with gap width of 90, 110 and 130 nm but at higher DC voltages. However, there was no current spike occurred for the feature of 160 nm gap width. A current spike indicates a dielectric breakdown or breakdown voltage from the body to the border since the DC voltage continuously applies to the body from 0.5 V until 100 V. The breakdown voltage occurred at lower voltage is more related to field emission of secondary ionization coefficient [4]. The breakdown voltages of the remaining features are shown in Table 2.

Table 2. The breakdown voltage for Binary reticle feature of 90 to 160 $\rm nm$

Feature gap width (Cr body to border) in nm	Breakdown voltage in Volts.
90	57.5
110	70.0
130	87.0
160	None

The breakdown voltage result of Table 2 was extrapolated for gap width of 10 to 250 nm as shown in Figure 5. The graph showed there is a linear relationship between the breakdown voltage and feature's gap width. The breakdown voltage for 160 nm gap width is expected within 108 to 116 Volts.

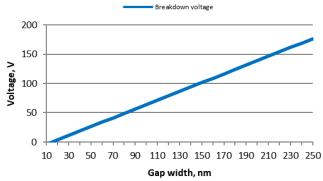


Fig 5. Breakdown voltage of nanometre scale gaps based on extrapolated data of 80 to 130 nm experimental quantification result

The experimental breakdown voltages were compared to international standard (indicated at ITRS) as showed in Figure 6. Its gradient is lower than the ITRS and voltage gap become wider and proportional to feature's metal-tometal gap width. Based on this finding, any CMOS semiconductor manufacturing which using international standards (ITRS and SEMI) may be at high risk of ESD damage to Binary reticle since the control limits are higher than the Binary reticle ESD threshold voltage.

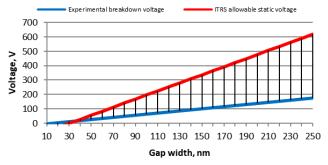


Fig 6. Breakdown voltage of experimental versus ITRS of Binary reticle

The voltage gap between experimental and ITRS for each gap width can be predicted using regression analysis.

The regression analysis is a set of statistical processes for estimating the relationships between a dependent variable. The voltage gap prediction was calculated using JMP statistical tool. The regression plot is shown in Figure 7.

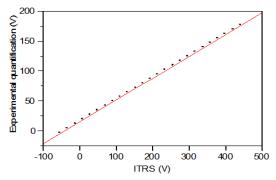


Fig 7. Regression plot of breakdown voltage of experimental and ITRS of Binary reticle

The correlation between experimental and ITRS breakdown voltage is R = 1 and the linear fit equation for experimental quantification voltage is V_{eq} = 15.772361 + (0.3647206 x V_{ITRS}). The voltage difference for each feature gap using the linear fit equation is shown in Table 3.

Table 3. The breakdown voltage comparison between experimental and ITRS for Binary reticle feature of 90 to 160 nm

Feature gap	Experimental	ITRS	Voltage	
width (Cr body	breakdown	breakdown	diffference	
to border) in nm	voltage (V1)	voltage (V2)	(V2-V1)	
90	57.5	114	57	
110	70.0	148	78	
130	87.0	195	108	

The experimental breakdwon voltage in Table 3 showed twice lower than ITRS. It is because the experimental breakdown voltage for each gap width was extrapolated from the ESD threshold voltage of 80 nm to 130 nm whereas ITRS using 1,000 nm feature [5]. The ITRS established the ESD threshold voltage in year 2003 which is the technology node use at that period of time.

The Binary reticle feature was inspected after direct discharge test to verify the ESD damage type. The ESD damage have 2 categories to date which is Pachen spark/sudden discharge and EFM [14], [15]. A microscope was used for inspecting it and the image of 80 nm feature is shown in Figure 8.

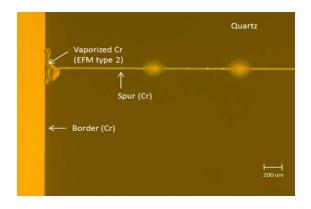


Fig 8. The 80 nm feature with EFM damage after direct discharge test

In Figure 8, the darker colour background is quartz. The quartz is transluscent but appeared as dark since it is laid

on microscope's black anodized base. The feature is shown in bright colour since it is made of Chromium (Cr) metal. The ESD defect image showed there were 3 locations in which vaporized metal occurred along the spur. The rainbow of colors emerged at these locations because the photoresist layer has peeled off due to the excessive heat after the high current passed through the metal and vaporized it thus resulting in multicolor depositions. The highest degree of vaporized metal was between spur and border. The fuse formation took place at this location before it later became vaporized after high current flew through the fuse. This ESD defect transformation is known as EFM and it occurred due to low voltage discharged. Similar EFM damage are observed at 90 nm and 110 nm.

Conclusion

The experimental quatification of ESD threshold voltage for Binary reticle of technology node < 250 nm revealed the breakdown voltage is actually twice lower than international standards (ITRS and SEMI) recommendation for CMOS semiconductor manufacturing. The ESD threshold voltage for Binary reticle using the extrapolation data of 80 nm to 130 nm is more accurate because the gradient is lower than the extrapolation data of 1,000 nm. The ITRS and SEMI should consider revising the electrostatic field allowable limit on reticle surface since its current recommendation is no longer accurate. There was no ESD damage at 160 nm gap width since 100 V direct discharge is insufficient to produce ionization path in between spur and border. However, based on the eperiment quantification result showed in Figure 5, the breakdown voltage of 160 nm gap width is 108 V.

The breakdown voltage for Binary reticle for both ITRS and experiment quantification showed linear relationship with nanometer metal-to-metal gap width which align with secondary ionization equation 2 and 3. The field emission from spur to body increases proportionally as the DC voltage to the spur increases until completed the ionization path between spur and body. The Binary reticle breakdown voltage at nanomter scale gap is influenced by Townsend-Fowler Nordheim secondary ionization.

The ESD defect for technology node < 130 nm are categorized as EFM based on Cr metal transformation as shown in Figure 8. Therefore, it is anticipated that Binary reticle of < 130 nm technology node are likely to be damaged by low voltage electrostic field.

Acknowledgments

The authors would sincerely like to express their gratitude and appreciation to Universiti Teknikal Malaysia Melaka (UTEM), SilTerra Malaysia Sdn. Bhd and Ministry of Higher Education (MOHE) for the research guidance and scholarship

Authors: Harriman Razman, SilTerra Malaysia Sdn Bhd, E-mail: harriman_razman@silterra.com; Associate Professor Dr. Azmi Awang Md Isa, Faculty of Electronic and Computer Engineering, Universiti Teknikal Malaysia Melaka, E-mail: azmiawang@utem.edu.my; Prof. Datuk Dr. Mohamad Kadim Suadi. Universiti E-mail: Malaysia Sarawak. kadim@cans.unimas.my

REFERENCES

- [1] Q. Wu, Y. Li, Y. Yang, S. Chen, and Y. Zhao, "The Law That Guides The Development of Photolithography Technology and The Methodology in The Design of Photolithographic Process," *China Semicond. Technol. Int. Conf. 2020, CSTIC 2020*, pp. 3– 8, 2020.
- [2] N. Mowell et al., "Criticality of Photo Track Monitoring for Lithography Defect Control," ASMC (Advanced Semicond. Manuf. Conf. Proc., vol. 2019-May, pp. 2019–2022, 2019.
- [3] M. A. Chik, A. B. Rahim, A. Z. M. Rejab, K. Ibrahim, and U. Hashim, "Discrete Event Simulation Modeling for Semiconductor Fabrication Operation," *IEEE Int. Conf. Semicond. Electron. Proceedings, ICSE*, pp. 325–328, 2014.
- [4] P. Jiang, M. Yuping, and H. Fang, "Photomask With Electrostatic Discharge Protection," US20200233298A1, 2020.
- [5] SEMI E163, "SEMI E163-0212 Guide For The Handling Of Reticles And Other Extremely Electrostatic Sensitive (EES) Items Within Specially Designated Areas," 2012.
- [6] G. Rider, "Why SEMI Standard E163 Should be Followed for The Protection of Extremely Electrostatic- Sensitive Semiconductors And Similar Devices During Manufacturing, Packaging And Handling," *Glob. Journals*, vol. 20, no. 3, 2020.
- [7] B. Billancourt and E. Souleillet, "Photomask and Method for Reducing Electrostatic Discharge on The Same itwh An ESD Protection Pattern," 2005.
- [8] J. Smallwood, "Can Electrostatic Discharge Sensitive Electronic Devices be Damaged by Electrostatic Fields?," J. Phys. Conf. Ser., vol. 1322, no. 1, 2019.
- [9] G. Rider, "Electrostatic Risks to Reticles and Damage Prevention Methodology," *Metrol. Insp. Process Control Microlithogr. XXX*, vol. 9778, no. March, p. 97782S, 2016.
- [10] L. Ledernez, F. Olcaytug, H. Yasuda, and G. Urban, "A Modification of Paschen Law for Argon," Int. Conf. Phenom. Ioniz. Gases, pp. 0–2, 2009.
- [11]A. Peschot, C. Poulain, N. Bonifaci, and O. Lesaint, "Electrical breakdown voltage in micro- and submicrometer contact gaps (100nm - 10µm) in air and nitrogen," *Electr. Contacts, Proc. Annu. Holm Conf. Electr. Contacts*, vol. 2015-Decem, pp. 280– 286, 2015.
- [12] A. Mayer, "Numerical Testing of The Fowler–Nordheim Equation for The Electronic Field Emission From A Flat Metal and Proposition for an Improved Equation," J. Vac. Sci. Technol. B, Nanotechnol. Microelectron. Mater. Process. Meas. Phenom., vol. 28, no. 4, pp. 758–762, 2010.
- [13] J. A. Montoya, L. Levit, and A. Englisch, "A Study of the Mechanisms for ESD Damage to Reticles," *IEEE Trans. Electron. Packag. Manuf.*, vol. 24–2, pp. 1–8, 2001.
- [14]G. C. Rider and T. S. Kalkur, "Experimental Quantification of Reticle Electrostatic Damage Below the Threshold for ESD," *Metrol. Insp. Process Control Microlithogr. XXX*, vol. 6922, pp. 69221Y-69221Y-11, 2008.
- [15]A. J. Wallash and L. Levit, "Electrical Breakdown and ESD Phenomena for Devices With Nanometer-to-micron Gaps," *Reliab. Testing, Charact. MEMS/MOEMS II*, vol. 4980, p. 87, 2003.
- [16] ITRS, "International Technology Roadmap Semiconductors -Factory Integration," in *International Technology Roadmap for Semiconductors 2011*, 2011.
- [17] SEMI E78, "SEMI E78-0912 Guide To Assess And Control Electrostatic Discharge (ESD) And Electrostatic Attraction (ESA) For Equipment," 2012.
- [18] SEMI E129, SEMI E129-0912 Guide To Assess And Control Electrostatic Charge In A Semiconductor Manufacturing Facility. SEMI, 2012.
- [19] H. Razman, A. A. M. Isa, W. A. A. W. Razali, M. K. Suaidi, and M. S. I. M. Zin, "A preliminary study of characterization techniques for reticle ESD threshold voltage measurement," *J. Telecommun. Electron. Comput. Eng.*, vol. 8, no. 1, pp. 53–57, 2016.
- [20] J. P. Howard, "Interpolation and Extrapolation," Comput. Methods Numer. Anal. with R, no. February, pp. 95–132, 2018.