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High Gain DC-DC Dual Converter integrating with Coupled Inductor and Diode Capacitor Switches

Abstract**:** *Many researchers have made great efforts to develop DC converter designs, to study how to increase voltage gain with low voltage stress and low ripple current. This paper proposed a DC-DC converter with a high conversion ratio, low voltage stress, and low ripple current based on the combination of two parallel boost converters. Using the interleaving approach, two converters, an inductor-coupled converter, and a conventional converter are connected on both sides of the input source to reduce the ripple of the source current, and the load is shared between them. Voltage gain and voltage stresses across power semiconductors were determined using steady-state analysis. In addition, Input current and output voltage ripple were analyzed. The inductors of this converter operate in continuous conduction mode (CCM). Higher voltage gain does not entail maximum duty cycle levels, which eliminates issues such as diode reverse recovery. The use of a passive clamp circuit reduces the voltage stress of the switch. This allows the use of low-voltage rated switches with low "on-case" impedance, which increases overall system efficiency. Theoretical analysis and mathematical relationships were performed. Finally, to validate the theoretical calculations, this converter was simulated in MATLAB / SIMULINK program. The results were good and largely identical to the theoretical calculations.*

Streszczenie: *Wielu badaczy włożyło wiele wysiłku w opracowanie konstrukcji konwerterów prądu stałego, aby zbadać, jak zwiększyć wzmocnienie napięcia przy niskim napięciu napięciowym i niskim prądzie tętnienia. W artykule zaproponowano konwerter DC-DC o wysokim współczynniku konwersji, niskim naprężeniu napięciowym i niskim prądzie tętnienia opartym na połączeniu dwóch równoległych konwerterów boost. Stosując podejście z przeplotem, dwa konwertery, konwerter sprzężony z cewką indukcyjną i konwerter konwencjonalny są połączone po obu stronach źródła wejściowego w celu zmniejszenia tętnienia prądu źródłowego, a obciążenie jest między nimi dzielone. Wzmocnienie napięciowe i naprężenia napięciowe w półprzewodnikach mocy określono za pomocą analizy stanu ustalonego. Ponadto przeanalizowano tętnienia prądu wejściowego i napięcia wyjściowego. Cewki indukcyjne tego przetwornika działają w trybie przewodzenia ciągłego (CCM). Wyższe wzmocnienie napięcia nie pociąga za sobą maksymalnych poziomów cyklu pracy, co eliminuje problemy, takie jak odzyskiwanie wsteczne diody. Zastosowanie pasywnego obwodu zaciskowego zmniejsza naprężenie napięciowe przełącznika. Pozwala to na stosowanie przełączników niskonapięciowych o niskiej impedancji „w obudowie", co zwiększa ogólną wydajność systemu. Przeprowadzono analizę teoretyczną i zależności matematyczne. Ostatecznie, aby zweryfikować obliczenia teoretyczne, konwerter ten został zasymulowany w programie MATLAB / SIMULINK. Wyniki były dobre iw dużej mierze identyczne z obliczeniami teoretycznymi.* (**Podwójny konwerter DC-DC o wysokim wzmocnieniu integrujący się ze sprzężonymi cewkami indukcyjnymi i przełącznikami kondensatorów diodowych**)

Keywords: High gain DC-DC Converter Coupled inductor, Current- ripple, Switches voltage stress
Słowa kluczowe: Przetwornica DC-DC o wysokim wzmocnieniu Sprzężona cewka, tętnienie prądu, naprężenie napięciowe

Introduction

In recent years, high voltage gain DC-DC boost converters have become increasingly important in a wide range of industrial applications, including uninterruptible power supplies, electric traction, and distributed solar cell (PV) generation technologies [1-4]. A traditional boost converter is typically utilized in these applications, however, the voltage stress of the main switches is equivalent to the high output voltage [5-6]. Due to the low voltage ranges generated by PV systems [7], which are renewable sources of energy are a popular topic [8-10]. As a result, the typical boost converter would be unsuitable for achieving high step-up voltage gain (Vout<8Vin) while maintaining high efficiency [11]. Several non-isolated structures have been developed in order to attain a high conversion ratio while avoiding running at extremely high duty cycles in the last ten years [6-12]. The cascaded approach [12-13], voltage-doubler or multiplier technique [14], are examples of non-isolated converters .coupled-inductor approach [15], switched-inductor and switched-capacitor approaches [16 - 17], capacitor-diode voltage multiplier [2]-[5]-[8], and voltage-lift technique [15-18] can achieve larger voltage gain than the voltage gain of a traditional boost converter with the required duty ratio. To produce high voltage gain, high frequency transformer-based direct voltage step-up [18 -19], the most of an interleaved coupled inductor, which allows for the use of smaller inductors, current split, and increased efficient inductance for high-voltage applications [20-22], passive and active clamped circuits are used in coupled inductor-based high gain converters to recover leakage energy and decrease leakage inductance losses [23-24]. The coupled inductor is used to boost the voltage level by utilizing the energy storage capabilities of the core's magnetizing inductance via the turn ratio of the coupled inductor [25]. Coupled inductor-based systems have the disadvantage of having larger leakage inductance, which generates voltage spikes across the main switch during turn-OFF and current spikes during turn-ON, leading to a drop in overall circuit efficiency. By employing an active clamp network, the consequences of leaking inductance may be minimized [23],

A double switch DC-DC converter with excellent voltage gain is proposed in this paper. The following are the specifications of the proposed converter:

(a) A coupled inductor efficient way increases the voltage gain, and the secondary winding of the coupled inductor is connected to a diode-capacitor to significantly the voltage gain.

(b) A passive clamped circuit is added to the coupled inductor's primary winding to reduce the voltage across the main switch to a smaller voltage level.

(c) As a result, reduced voltage rating and lower closed-state resistance RDS (ON) power components can be chosen. This diode–capacitor circuit, is effective for improving the voltage conversion ratio. The coupled inductor's leakage inductance energy may be recycled, then increasing efficiency.

(d) By incorporating coupled inductor converters with non-coupled inductor converters and employing switch capacitor-diode and switch inductor-diode, it is possible to obtain converters with very little voltage stress on the switches in comparison to the output voltage, and the resulting conversion ratio does not depend solely on the duty ratio due to the presence of the winding ratio (n). The description of the proposed converter is given in Section 2. Section 3 describes the steady-state and basic operation of

the proposed converter and describes the proposed converter's design procedure. Section 4 displays the result waveforms for the proposed
(e) converter's important components using the MATLAB/SIMULINK program for the data presented in Table I. Finally, Section 5 provides the conclusion.

1. onstruction of the proposed converter

The proposed high gain dc-dc converter shown in Figure 1 consists of two converters connected in parallel on both sides of the input source. The first converter consists of the coupled inductor (L1, L2), passive clamp circuit, and intermediate capacitor C2 .this section connected in parallel to the second converter consists of the uncoupled conventional boost converter connected in series with voltage multiplier cell to boost output voltage and auxiliary inductor to avoid reverse diode problem and reduce switches stress. The voltage applied to the circuit is denoted by the symbol Vin, S1 is the main switch, a coupled inductor's primary and secondary inductors are designated by the letters L1 and L2, respectively.

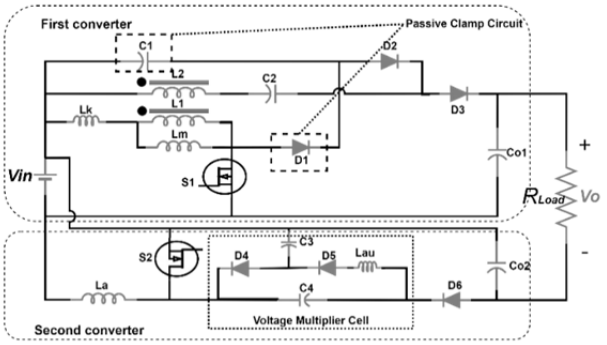


Fig. 1. The schematic graph of the proposed converter

The passive clamp network over L1 is represented by C1 and D1. The output capacitor is Co1, and the output diode is D3. On the second inductor L2, C2 operates as an auxiliary energy storage capacitor, while D2 operates as a feedback diode. Where VL1 and VL2 are the voltages across coupled inductors L1 and L2, respectively. On the other side, S2 is the second main switch. The uncoupled inductor is represented by La .the voltage multiplier is connected to La represented by C3, C4, D4, D5, and the auxiliary inductor is denoted by Lau. Where VLa and VLau are the voltages across inductor La and Lau respectively. The output capacitor Co2, and the output diode D6.Vo represents the average output voltage (dc) across the load.

Stead state assumptions

The following assumptions are assumed in this section to simplify the analysis:

- All of the components are considered to be ideal.
- The voltages of capacitors remain constant.
- Input voltage is constant.
- The parasitic resistance of connected inductors and the ESR of capacitors are ignored.
-

Operational modes

The continuous conduction mode (CCM) operating modes are given in Fig. 3. Included below are the different operating modes. In CCM mode, this converter has six operational modes. These modalities are discussed in the subsections that follow. Figures 2 and 3 depict the operational modes and significant waveforms. The switches' duty cycles are equal to or greater than 0.5 (D≥0.5) and the same procedure when the converter operates under duty cycles is less than 0.5.

Mode 1 ($t_o \le t \le t_1$):

At startup, switch and switch S2 is turned ON. In the first converter (coupled inductor), current passes through the switch S1 and is fed to the primary side of the coupled inductor (L1), energizing the coupling magnetizing inductance (Lm). The two diodes, D1 and D3, are reverse biased during this mode. The secondary inductor L2 and capacitor C1, charge C2 via D2. In the second converter (uncoupled inductor), the energy at the inductor La increases. Capacitor C3 charges both the auxiliary inductor Lau and capacitor C4 during the path S2- C4- Lau-D5. Diode D4 and D6 are reverse biased. The paths of currents for mode 1 are as shown in Figure 2 and the equations for the currents are as follows:

(1) $$I_{Lm} = \frac{V_{in}}{L_m + L_k}\,(t - t_0) + I_{Lm}(t_o)$$

(2) $$I_{La} = I_{La}(t_o) + \frac{V_{in}}{L_a}.(t - t_o)$$

(3) $$I_{L_{au}}(t) = I_{L_{au}}(t_o) + \frac{V_{C3} - V_{C4}}{L_{au}} \cdot (t - t_0)$$

Mode 2: $t_1 \le t \le t_2$

This mode switch S1 is still ON and S2 is turned OFF. The inductor coupled on the first converter has the same position as mode1. On the other side, the power in the inductor La decreases. The energy stored in the auxiliary inductor Lau slowly decreases. The capacitors C3 and Co2 are charged by the energy stored in the inductor La through D4 and D6 respectively. The paths of currents for mode 2 are as shown in Figure 3 and the equations for the currents are as follows

(4) $$I_{Lm} = \frac{V_{in}}{L_m + L_k}\,(t - t_1) + I_{Lm}(t_1)$$

(5) $$I_{La} = I_{La}(t_1) + \frac{V_{in} - V_{C3}}{L_a}.(t - t_1)$$

(6)

$$I_{L_{au}}(t) = I_{L_{au}}(t_1) + \frac{V_{C3} - V_{C4}}{L_{au}} \cdot (t - t_1)$$

Mode 3: $t_2 \le t \le t_3$

This mode switch S1 is still turned ON and switch S2 is still turned OFF. The coupled inductor on the first converter of the proposed converter has the same mode 2. On the other side, the energy decreases continuously in the inductor La. When consuming the stored energy in auxiliary inductor Lau, diode D5 is reverse biased and this advantage for it avoids diode reverse recovery problems and decreases electromagnetic interference. The paths of currents for mode 3 are as shown in Figure 4 and the equations for the currents are as follows:

(7) $$I_{Lm} = \frac{V_{in}}{L_m + L_k}\,(t - t_2) + I_{Lm}(t_2)$$

(8) $$I_{La} = I_{La}(t_2) + \frac{V_{in} - V_{C3}}{L_a}.(t - t_2)$$

(9) $$I_{L_{au}}(t) = o$$

Mode 4: $t_3 \le t \le t_4$

This mode switch S1 remains ON and the S2 switch is turned ON. The coupled inductor on the first converter and the uncoupled inductor on the second converter has the same mode 1.

Mode 5: $t_4 \le t \le t_5$

This mode switch S1 is turned OFF and the switch S2 remains ON. In the coupled inductor on the first converter, the leakage energy on the primary side of the coupled inductor (L1) is returned to the clamp capacitor (C1) via D1. The current in D2 is zero because it is reverse biased. Diode D3 is forward biased in this mode and also transfers power from the input

to the output side. On the other side. The uncoupled converter has the same action for mode 4. The paths of currents for mode 5 are as shown in Figure 5 and the equations for the currents are written as follows

(10) $$I_{Lm} = \frac{V_{C1}}{L_m + L_k}\,(t - t_4) + I_{Lm}(t_4)$$

(11) $$I_{La} = I_{La}(t_4) + \frac{V_{in}}{L_a}.(t - t_4)$$

(12) $$I_{L_{au}}(t) = I_{L_{au}}(t_4) + \frac{V_{C3} - V_{C4}}{L_{au}} \cdot (t - t_4)$$

Mode 6: $t_5 \le t \le t_6$

This mode switch S1 is still OFF and the S2 switch is still ON. In the coupled inductor on the first converter, after the leakage power recovery from the inductor L1, is completed, the capacitor C1 is fully charged, and then D1 is reverse biased, at the same time D2 remains to reverse biased. The uncoupled converter has the same mode 5. The paths of currents for mode 6 are shown in Figure 6 and the equations for the currents are written as follows:

(13) $$I_{Lm} = \frac{(V_{Co1} - V_{c2} - V_{in})}{n(L_m + L_k)}\,(t - t_5) + I_{Lm}(t_5)$$

(14) $$I_{La} = I_{La}(t_5) + \frac{V_{in}}{L_a}.(t - t_5)$$

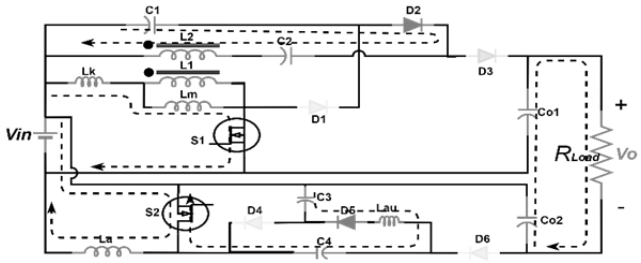


Fig 2. Equivalent circuits in mode 1&mode 4

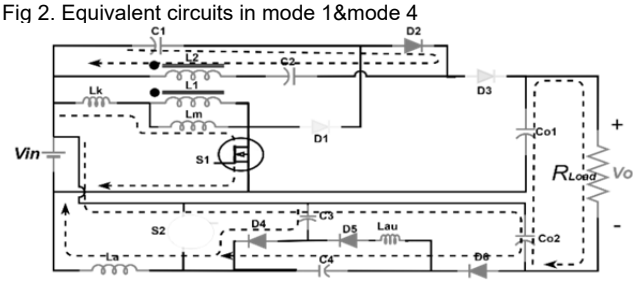


Fig 3.Equivalent circuits in mode 2

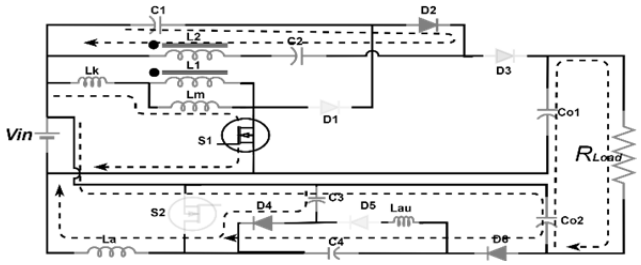


Fig 4. Equivalent circuits in mode 3

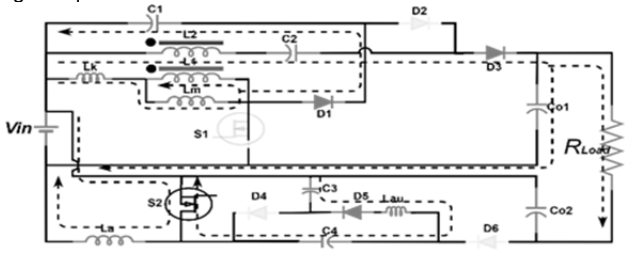


Fig 5. Equivalent circuits in mode 5

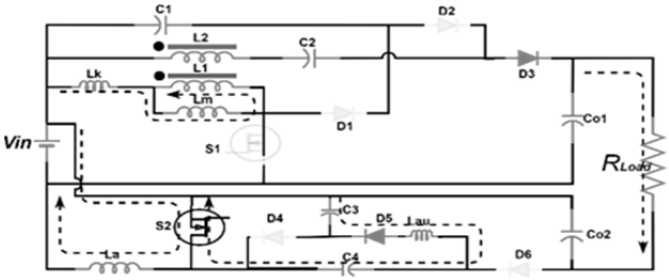


Fig 6. Equivalent circuits in mode 6

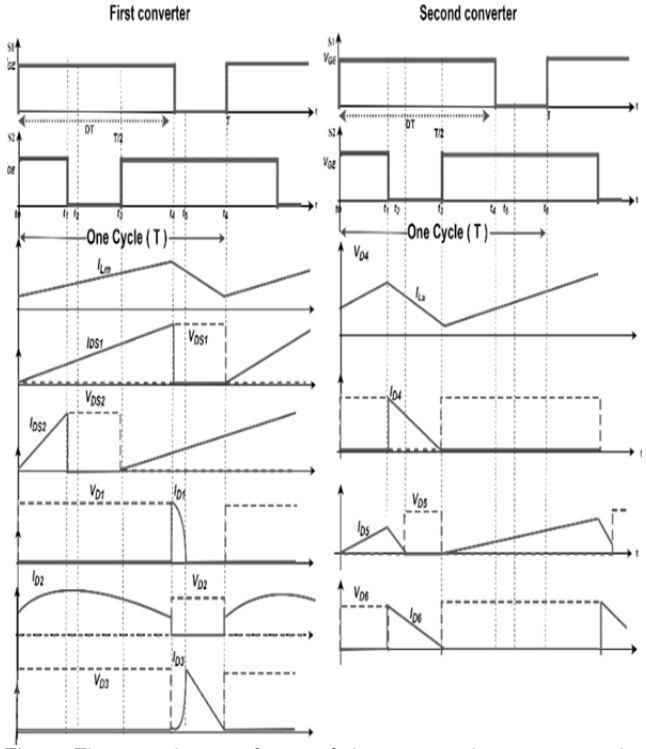


Fig 7. The sample waveforms of the proposed converter under steady-state operation.

Theoretical analysis

This section discusses the proposed converter's analysis, which may be utilized to help in its design.

When Switch S1 and Switch S2 are ON

The voltage across L1, L2, La, and Lau is given by

(15) $$V_{L1} = V_{in}$$

(16) $$V_{L2} = V_{c2} - V_{c1}$$

(17) $$V_{L2} = nV_{in};\ where\ \ turn\ ratio\ , n = \frac{V_{L2}}{V_{L1}} = \frac{\sqrt{L2}}{\sqrt{L1}}$$

(18) $$V_{La} = V_{in}$$

(19) $$V_{Lau} = V_{c3} - V_{c4}$$

When Switch S1 and Switch S2 are OFF

The voltage across L1, L2, La, and Lau are voltage given by

(20) $$V_{L1} = -V_{c1}$$

In Mode 5, use Kirchhoff's voltage law

(21) $$V_{L2} = V_{in} + V_{c2} - V_{co1}$$

From Eqs. 13,14,15, and 21, the voltage VL1 during switch-off becomes

(22) $$V_{L2} = V_{in} + nV_{in} - V_{L1} - V_{co1}\ ; V_{L1} = \frac{V_{L2}}{n}$$

(23) $$V_{L1} = \frac{V_{in}(1+n) - V_{co1}}{n+1}$$

(24) $$V_{La} = V_{in} - V_{c3}$$

(25) $$V_{Lau} = 0$$

Voltage gain calculation

By balancing the voltage-sec across L1

(26) $$V_{L1(S1\ ON)} + V_{L1(S1\ OFF)} = 0$$

Form Eqs. 13 and 23

(27) $$V_{in}.D + \frac{V_{in}(1+n)-V_{co1}}{(n+1)}.(1-D) = 0$$

(28) $$V_{co1} = \frac{(n+1)}{1-D}.V_{in}$$

By balancing the voltage-sec across La

(29) $$V_{La(S2\ ON)} + V_{La(S2\ OFF)} = 0$$

Form Eqs. 16 and 23

(30) $$V_{C3} = \frac{V_{in}}{1-D}$$

By balancing the voltage-sec across Lau

(31) $$V_{Lau(S2\ ON)} + V_{Lau(S2\ OFF)} = 0$$

Form Eqs. 19 and 25

(32) $$V_{c4} = V_{c3} = \frac{V_{in}}{1-D}$$

Also applying the KVL law in the loop V_{c3}- V_{c4} -V_{co2}, the following equation could be obtained

(33) $$V_{co2} = V_{c3} + V_{c4} = \frac{2V_{in}}{1-D}$$

And applying the KVL law in the cycle V_{in} -V_{co1}-V_o - V_{co2}, the following equation could be obtained

(34) $$V_o = V_{co1} + V_{co2} - V_{in}$$

By substituting (29), and (34) in (35) the voltage gain is

(35) $$\frac{V_o}{V_{in}} = \frac{n+2+D}{1-D}$$

Voltage stress calculation

The voltage stresses across each of the switches can be calculated as follows

(36) $$V_{S1} = -V_{L1(S1\ OFF)} + V_{in}$$

From Eqs.23,29,and 37

(37) $$V_{S1} = \frac{V_{in}}{1-D}$$

By applying the KVL law in mode 2 in loop S2–C3–D4, the following equation could be obtained

(38) $$V_{S2} = V_{c3}$$

From Eqs. 31, and 39

(39) $$V_{S2} = \frac{V_{in}}{1-D}$$

The voltage stresses across the diode D1

(40) $$V_{D1} = V_{L1(S1\ ON)} + V_{c1}$$

The voltage across the clamp capacitor, C1, is essentially constant for the whole switching time

From Eqs.15,and 20

(41) $$V_{c1} = \frac{D}{1-D}.V_{in}$$

From Eqs.15,41,and 42

(42) $$V_{D1} = \frac{V_{in}}{1-D}$$

The voltage across the diode D2

(43) $$V_{D2} = V_{L2} + V_{c2} - V_{c1}$$

From Eqs.22,23,and 29

(44) $$V_{D2} = 2nV_{in}$$

Thevoltage across the diode D3

(45) $$V_{D3} = V_{L2} - V_{c2} - V_{in} + V_{co1}$$

From Eqs.16,17,and 46

(46) $$V_{c2} = \frac{n+(1-n).D}{1-D}.V_{in}$$

From Eqs.17,29,46,and 47

(47) $$V_{D3} = \frac{n}{1-D}.V_{in}$$

The voltage across the diode D4

(48) $$V_{D4} = V_{c3}$$

From Eq.31

(49) $$V_{D4} = \frac{V_{in}}{1-D}$$

The voltage across the diode D5

(50) $$V_{D5} = V_{c4}$$

From Eq.33

(51) $$V_{D5} = \frac{V_{in}}{1-D}$$

The voltage across the diode D6

(52) $$V_{D6} = V_{c3}$$

From Eq.28

(53) $$V_{D6} = \frac{V_{in}}{1-D}$$

Design procedure

Inductors design

To calculate the minimum value of the inductance to be the converter in (CCM) operating let's assume the proposed converter operating in (BCM) boundary conduction mode and lossless condition.

(54) $$I_{Lm(\max)} = \Delta I_{Lm}$$

(55) $$I_{Lm(\min)} = 0$$

(56) $$I_{inav} = \frac{\Delta I_{Lm}}{2}$$

where $ILm(max)$ and $ILm(min)$ are maximum and minimum current in magnetizing inductance and ΔI_{Lm} is ripple currents. According to the balance of input and output power.

(57) $$I_{inav} = \frac{V_O I_O}{V_{in}}$$

(58) $$L_{m(min)} = \frac{V_{in}.D.T_S}{I_{Lm(\max)}}$$

From Eqs.36,59,and 60

(59) $$L_{m(min)} = \frac{R_L}{2}.\left(\frac{1-D}{2+n+D}\right)^2.DT_S$$

Where RL is the load resistance. The same procedure for La

(60) $$L_{a(min)} = \frac{V_{in}.D.T_S}{I_{La(\max)}}$$

(61) $$L_{a(min)} = \frac{R_L}{2}.\left(\frac{1-D}{2+n+D}\right)^2.DT_S$$

To design the inductor Lau, keep in mind that when the switch S2 is turned on an approximate voltage at the two terminals of the auxiliary inductor can be obtained as follows:

(62) $$V_{Lau} \approx \frac{\Delta V_{C3}+\Delta V_{c4}}{2}$$

(63) $$L_{au(min)} = \frac{V_{Lau}.D.T_S}{\Delta I_{Lau}}$$

Capacitors design

The clamping capacitor C1's minimum value may be calculated as follows:

(64) $$C_1 \approx \frac{I_m.d_1.T_S}{\Delta V_{c1}}$$

Where $(d_1.T_S)$ is duration operation for mode 5($t_4 \le t \le t_5$), that current flows through the capacitor C1 in this period. The following equation can be used to calculate the minimum value of the intermediate capacitor C2

(65) $$C_2 \approx \frac{I_m.DT_S}{n.\Delta V_{c2}}$$

During a switching cycle (DT), the output capacitors Co1 and Co2 must deliver the output load current. Because the output capacitors are connected in series, each capacitor value for a voltage variation of ΔVo during a specified interval might be calculated as follows

(66) $$C_{o1} = C_{o2} \approx \frac{I_0.DT_S}{n.\Delta V_{Co1,2}}$$

For a period (D T), the current that flows through the capacitor C3 is half the average input current and the variable voltage $\Delta VC3$ on it can be calculated

(67) $$\Delta V_{C3} = \frac{1}{C_3}\int_0^{DT_S}\frac{I_{inav}}{2}dt$$

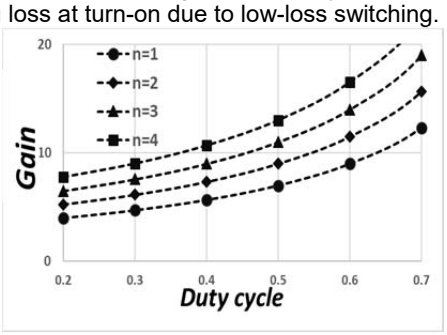
(68) $$C_3 = \frac{I_{inav}}{2\Delta V_{C3}} . DT_S$$

Similarly, the capacitor C4, has the same design equation

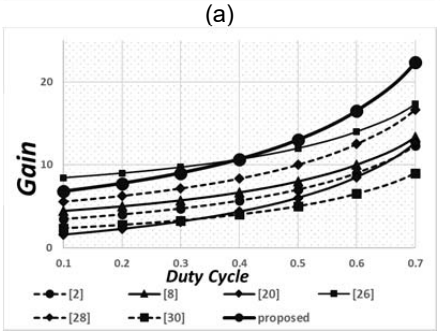
(69) $$C_4 = \frac{I_{inav}}{2\Delta V_{C4}} . DT_S$$

Review of comparison

A selection of DC-DC converters with high conversion and lower power voltage stresses has been chosen for comparison with the proposed converter. Table 1 compares the major characteristics of the converters, such as the number of components, voltage gain, switch voltage stress, and maximum diode voltage stress. Figure 8 shows the gain compared to many homothetic converters. Figure 9 displays a voltage stress comparison of the switching device when all converters and proposed converters are equal in turn ratio. The pattern is shown in Figure 8 (a) and (b) suggest using a turn ratio of divalent turn ratios of about 4 or 5 (fixed throughout the design process). For the inductor, adjusting the duty ratio between 0 and 0.7 during operation would be a reasonable way to build and operate the proposed converter. The losses increase dramatically above this range of duty cycle and turn ratio. The ability to produce high voltage gain without utilizing severe duty cycle ranges is a significant benefit versus conventional boost converters. One of the causes of the proposed converter's good efficiency is the decrease in switching loss at turn-on due to low-loss switching.

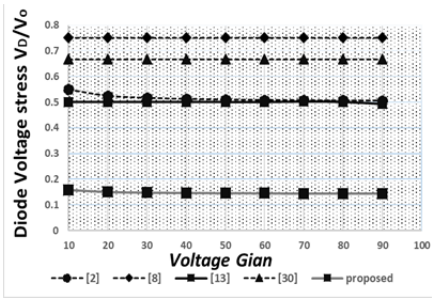


(a)

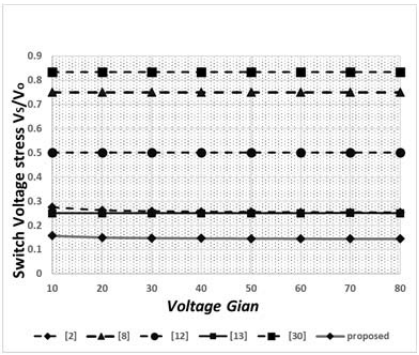


(b)

Fig 8. (a). Gain vs. duty cycle for various turn ratios n. (b) Comparison of voltage gains with n=4.



(a)

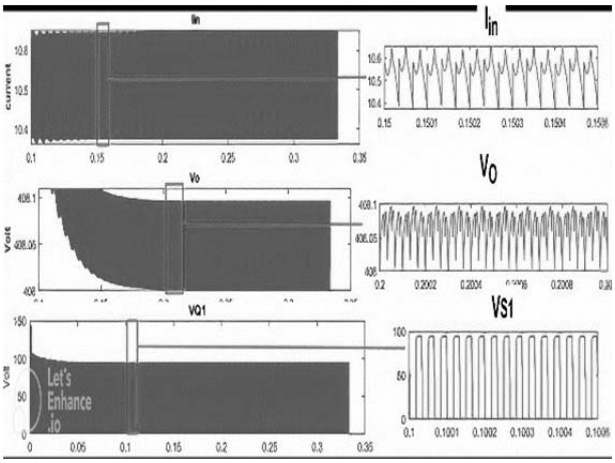


(b)

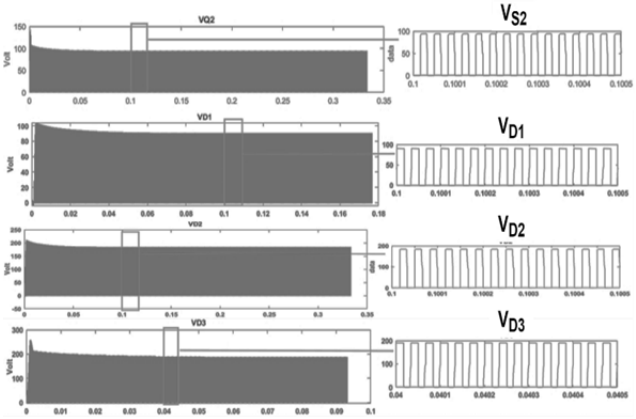
Fig 9. **(a)**Diode voltage stress compassion as a ratio to output voltage for turn ratio (n=4)**(b)** Switch voltage stress compassion as a ratio to output voltage for turn ratio (n=4)

Simulation results

Figure 10,11,and Figure 12 depicts the simulation results' waveforms for the same parameters given in Table 2, which shows the current flowing through the primary of the coupled inductor (L1) and the waveforms of the clamp and intermediate diodes, as well as other waveforms of diodes . Table 3 shows the similar near results between the analytical calculation and simulation results.

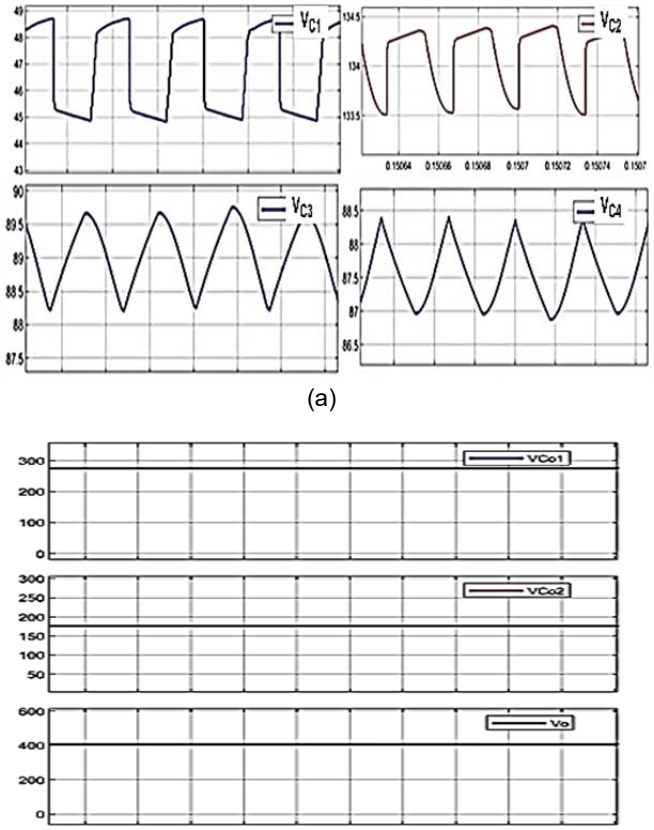


(a)



(b)

Fig 10. **(a)**Input current ripple,output voltage ripple,and voltage stress S1 waveform. **(b)** Voltage stress S2,voltage stress D1,D2,and D3 waveforms.



(a)

(b)

Fig 12. **(a)**Voltage capacitors C1,C2,andC3 **(b)** Voltage output capacitorsCo1, Co2,and Output voltage waveforms

Table 2. Converter component and parameters utilized

arameter name	Value
Input voltage	45 V
Output voltage	400 V
Output power	400 W
Duty cycles	50%
Switching frequency	30 kHz
Input inductors	400μH
Auxiliary inductors	5μH
Coupled inductor(Lm)	50 μH
Turns ratio of the coupled Inductor (n)	2
Capacitors C1	1 μF
Capacitors C2	47 μF
Capacitors C3~ C4	25μF
Co1 and Co2	180μF

Table 3. Similarities in analytic and simulation results

Parameters	Formula	Analytical Results	Simulation Resultsarisons
Voltage across C1	$V_{c1} = \frac{D}{1-D}.V_{in}$	45v	46.5v
Voltage across C2	$V_{c2} = \frac{n+(1-n).D}{1-D}.V_{in}$	135v	134.75v
Voltage across C3	$V_{C3} = \frac{V_{in}}{1-D}$	90v	89.5v
Voltage across C4	$V_{C4} = \frac{V_{in}}{1-D}$	90v	88v
Reverse voltage across D1	$V_{D1} = \frac{V_{in}}{1-D}$	90v	88v
Reverse voltage across D2	$V_{D2} = 2nV_{in}$	180v	185v
Reverse voltage across D4,5,6	$V_{D4,5,6} = \frac{V_{in}}{1-D}$	90v	89v
Reverse voltage across switch S1,2	$V_{S1,2} = \frac{V_{in}}{1-D}$	90v	90.7v
Voltage across Co1	$V_{co1} = \frac{(n+1)}{1-D}.V_{in}$	270v	269v
Voltage across Co2	$V_{co2} == \frac{2V_{in}}{1-D}$	180v	179v
Output voltage Vo	$V_O = \frac{n+2+D}{1-D}.V_{in}$	405v	400v

4. Conclusion

In this paper, a conventional converter conected to diode capacitor switch and combined with coupled inductor converter in a parallel to produce a high-gain DC-DC equivalent converter. When it compared with the traditional converter, the proposed converter has the following advantages.

1) The gain ratio can be obtained by configuring the coupling inductor turn ratio and duty cycle, which can be effective. This can avoid too high a duty cycle and reduce the leakage inductance loss caused by aweak surge coupling frequency converter.
2) The voltage multiplier circuits have increased the gain ratio, which reduces the duty cycle range and thus reduces stress on the converter elements.

The steady-state analysis of the proposed converter, such as the voltage gain, voltage stress on the switching device, is presented. The characteristics are designed to demonstrate the superiority of the proposed converter. Finally, the data are given in the second table are used to simulate calculations by using the MATLAB / SIMULINK program and are very close to theoretical calculations.

Table 1. Characteristics comparison

Parameter name	[2]	[8]	[12]	[13]	[22]	[26]	[28]	[30]	proposed
Coupled inductor	*No*	*Yes*	*Yes*	*No*	*Yes*	*Yes*	*Yes*	*Yes*	*Yes*
No.of capacitors	3	3	2	5	4	4	4	5	6
No.of Diodes	3	3	4	5	4	5	4	6	6
No.of switches	2	2	2	2	1	2	2	2	2
Voltage gain $\frac{V_O}{V_{in}}$	$\frac{3+D}{1-D}$	$\frac{4}{1-D}$	$\frac{2(1+nD)}{1-D}$	$\frac{4}{1-D}$	$\frac{1+n}{1-D}$	$\frac{n(2-D)}{1-D}$	$\frac{1+n}{1-D}$	$\frac{2+n}{1-D}$	$\frac{n+2+D}{1-D}$
Stresses of diodes	$\frac{V_O+V_{in}}{2}$	$\frac{V_O}{4}, 3\frac{V_O}{4}$	nV_{in}	$\frac{-2V_{in}}{1-D}$	$\frac{nV_O}{1+n}$	$V_O - nV_{in}$	$\frac{nV_{in}}{1-D}$	$\frac{nV_O}{2+n}$	$\frac{V_{in}}{1-D}$
Stresses of switches	$\frac{V_O+V_{in}}{4}$	$\frac{V_O}{4}, 3\frac{V_O}{4}$	$\frac{V_O}{2}$	$\frac{V_{in}}{1-D}$	$\frac{V_O}{1+n}$	$\frac{\frac{V_O}{n}-V_{in}}{2}$	$\frac{V_{in}}{1-D}$	$\frac{(n+1)V_O}{2+n}$	$\frac{V_{in}}{1-D}$

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