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Low Power Dynamic Comparator design in 90nm technology

***Abstract**. This work proposes a dynamic comparator design for biomedical signal acquisition. The circuit consumes 4.598uW of power and the propagation delay is found as 39.26ps.The offset voltage variation is 1.33mV, which is the best amongst contemporary designs. The design is simulated using 90nm CMOS scale technology. The designed circuitry of the system is having only 11 number of transistors which make the system more optimised for real time application. The layout area of the design is found as 20.76um^2.The circuit is simple, linear and area efficient and this makes it suitable for low power applications.*

Streszczenie.** W tej pracy zaproponowano projekt dynamicznego komparatora do akwizycji sygnału biomedycznego. Obwód zużywa 4,598 uW mocy, a opóźnienie propagacji wynosi 39,26 ps. Zmienność napięcia przesunięcia wynosi 1,33 mV, co jest najlepszym wynikiem wśród współczesnych projektów. Projekt jest symulowany przy użyciu technologii skali CMOS 90 nm. Zaprojektowany obwód układu ma tylko 11 tranzystorów, co sprawia, że układ jest bardziej zoptymalizowany do zastosowań w czasie rzeczywistym. Powierzchnia układu projektu wynosi 20,76 um2. Obwód jest prosty, liniowy i efektywny powierzchniowo, dzięki czemu nadaje się do zastosowań o niskim poborze mocy.* (Konstrukcja komparatora dynamicznego małej mocy w technologii 90nm***)

eywords: SAR ADC, Dynamic comparator, Low power, Dual-tail comparator design, Bio-physiological signals.
Słowa kluczowe: komparator, technologia 90 nm.

Introduction

Dynamic comparators are one of the major circuits in the field of data convertors (Analog to Digital) [1].To reduce the average power consumption of an ADC, the individual blocks have to consume optimal power. Earlier, static comparators were used for this purpose. In low power arena the static design is not preferred due to static power consumption. In recent times, these are replaced by dynamic comparators (Fig.1) due its inherent low power capability. It is having two stages, namely i) Initial amplification stage (Pre-amp) and the ii) decision making stage or latching stage. The signals to be compared is applied to the amplification phase. The differential output from the amplifier is used to drive the decision making stage(latch stage).The latching stage is an inverted back to back arrangement which gives the comparison result.

In the biomedical field, patient's health condition is monitored digitally now-a-days. Implantable devices like pace-maker etc. remains in contact with important organs and collects vital signal informations.These signals are generally being processed digitally for diagnostic purpose. The implantable devices are battery-powered devices and an in efficient design may draw larger power and the battery may get drained off suddenly. This may critically affect the health condition of the patient.

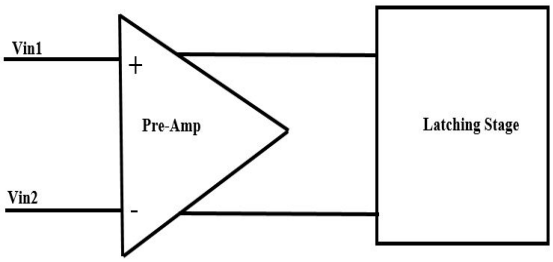

Fig.1.Blocks of dynamic comparator

To increase the durability of the design, it must consume least average power. Low power techniques can be incorporated with the circuit to achieve this target. In fact, additional circuits increase the design complexity and area. In biomedical applications, along with power, area is also to be kept minimum. The design proposed in [2] is effective in high speed comparison at the cost of large offset variation. In [3], the circuit consumes less power by adaptive working.Extra controlling circuit is incorportaed to achieve low power which makes the design bulky. A comparator design for biomedical applications is given in[4].Though the design achieves better power performance, the non-linearity factor increases. Moreover, more number of transistors are used for the circuit implementation.

In medical applications,a low power,less complex comparator is prefered.The rest of the paper is organised as follows.Section 2 deals with the existing dynamic comparator design.Section 3 describes the propsed circuit.The results and discusssions are included in section 4 and section 5 concludes the work.

Existing related works

Fig.2 shows a dual-tail two stage comparator design [5,6].

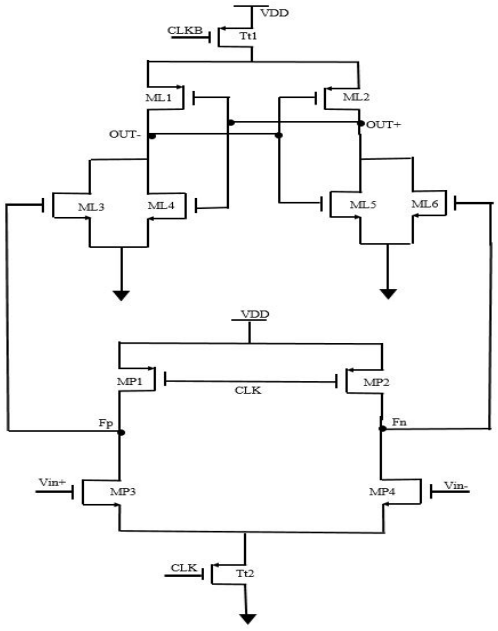

Fig.2.Conventional dual tail comparator

In the conventional circuit two stages are used.The initial amplification stage is also known as the input stage.The signals to be compared are applied in this stage(Vin+,Vin-).The dual-tail methodlogy is followed here (Tt1 and Tt2 are the tail MOSFETes). Tt1 is wide enough to pass more current to latching stage to speed up the decision making operation. Latching stage is made of two back to back connected invertors. When the clock signal (CLK=0),the circuit enters in to the amplification stage. Both Tt1 and Tt2 are OFF and transistors TP1 and TP2 in the bottom half of the design turn ON.The nodes Fp and Fn charge to VDD. The high value at Fn and Fp transistors turns on transistors ML3 and ML6.The two output nodes OUT+ and OUT- are discharged to GND.This is the initial condition or the resetting operation.The senond phase is known as decision making phase.Here,the clock(CLK =1) is made high.The Tt1 and Tt2 are ON under this condition.The output terminals(Fn and Fp) start discharging to GND.The rate of discharging of these two nodes differ by the inputs that are being applied (Vin+ and Vin-).When Vin+>Vin-,then Fp node discharges faster than Fn.This creates a differential input voltage(∆Vin) across Fn and Fp.This voltage difference is transfered to the latch stage through ML3 and ML6.Finally,OUT- node settles to VDD and the OUT+ node is pulled down to GND.

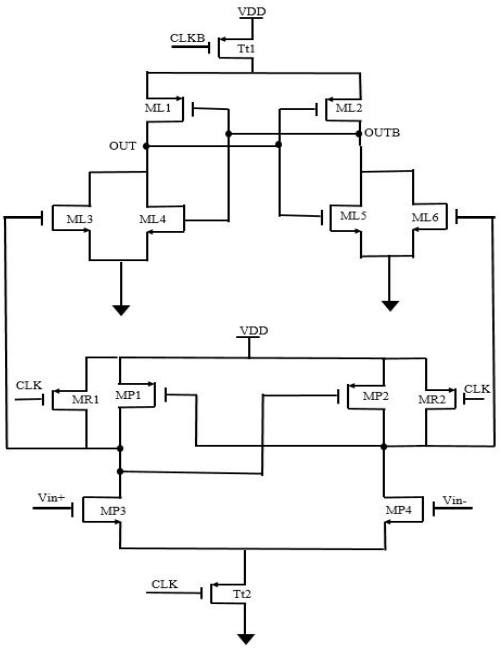

Fig.3.Dual Tail comparator with modified amplifier stage.

In Fig.3, an improvised version of the dual-tail comparator is presented [7].The MP1 and MP2 transistors are connected back to back.The operation of the circuit is similar to the circuit given in Fig.2. This,in fact, increases the gain of the ampification process.This increases the positive feed backing of the latching stage,which in turn improves the speed of the design.Additionally, transistors, MR1 and MR2 are added in the circuit, which improves the controllability.Although the circuit speed is improved,the power consumption and area requirement of the design is still high.The offset voltage,which is a lineraity measure of the design is 7.8mV.The design consumes 360uW of power.

Static power consumption is one of the main draw backs of the aforementioned design.To reduce this an alternate design approch can be adopted from [8]. Two additional transiors (Mst1 and Mst2 are incorporated in the amplification stage. (Fig.4).These transistors are instrumental in reducing the static current throuth the circuit and effectivelty reduces the total power consumption.The circuit dissipates an average power of 132.41uW.

In low power VLSI design,atmost importance is given to the power consumtion.Along with power consumption,

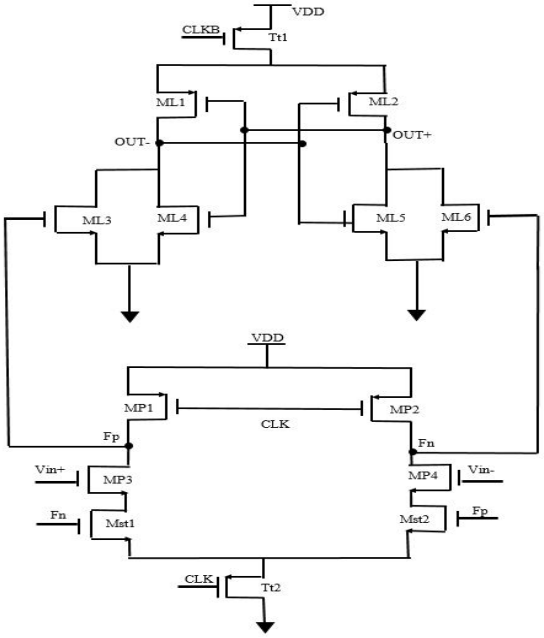

Fig.4.Conventional dual tail comparator improved

methods to reduce the complexity of the design can also be incorporated.Thus,a power and area efficient system can be achieved.

Proposed Comparator

The main objective of this study is to design a dynamic comparator suitable for biological signal acquisition system.Keeping this in mind, the first intention is to achieve low power consumption.The strategy adpoted in this design is to realise the circuit with less number of transistors.

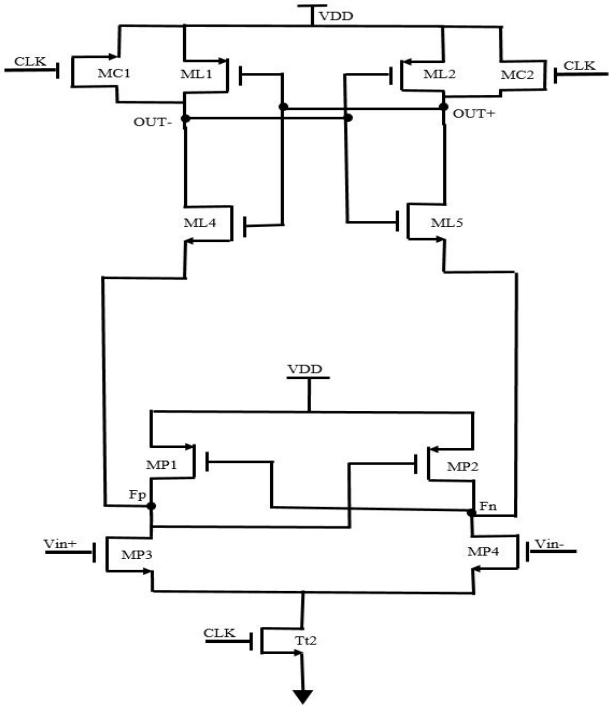

Fig.5. Proposed comparator schematic

The circuit of the propsed design is given in Fig.5.Here,a one-tail double stage methodology is used.The mode of connection used to interconnect the initail amplification stage to the latching state is also different from the conventional architectures.The drain terminals of transitors ML4 and ML5 are directly connected to the Fp and Fn nodes of the amplification stage.The ML3 and ML6 transtors are removed from the design. Similarly,intermediary transostors MR1 and MR2 from Fig.3 are also removed in the new design.This helps to reduce the capactive mismatch effect in total and leads to effectively reducing the offset error.The upper-tail (Tt1) transistor is removed in the new design.The clock distribution network of this design is only having CLK signal.The complementary clock signal (CLKB) is not required for its operation.The reduction of clock load helps the design to consume less average power.In the amplification stage,the Fn node is fed back to the gate of MP1 and Fp node is fed back to the gate of MP2 transistor.This feedbacking helps to maintain high gain,since the input voltage difference(ΔVin) keeps on increasing exponentially with the the differential inputs.This high gain improves the latching speed.The operation of the circuit is given below.

When the clock is low , the transistors MC1 and MC2 will be ON and the Tt1 transistor is OFF.The output nodes,OUT+ and OUT- charged to high voltage.This is the initial or pre-setting condition.The second phase of operation is the decision making,where the comparator outputs become high or low depending on the applied input signals.Ths is acheived by making the clock signal high(CLK=1) which makes the tail transistor ON.The signals to be compared are applied to Vin+ and Vin- respectively.These applied signals enables the input transistors(MP3 and MP4).The output nodes of the latching stage will start discharging through nodes Fn and Fp according to the applied input signals.

Consider the condition,Vin+ > Vin-, then the MP3 transistor conducts heavily compared to MP4.As a result OUT- node discharges faster than the OUT+node.Tis node finally discharged to GND.This low voltage at OUT- switches of the ML5 transister and switches ON the ML2 transistor(both these transistors are part of the inverter arrangement in the latching stage).Thus,the OUT+ node is pulled to the high vaue(VDD) and the compartor has made a decision.Comparator's output is given in Fig.6.

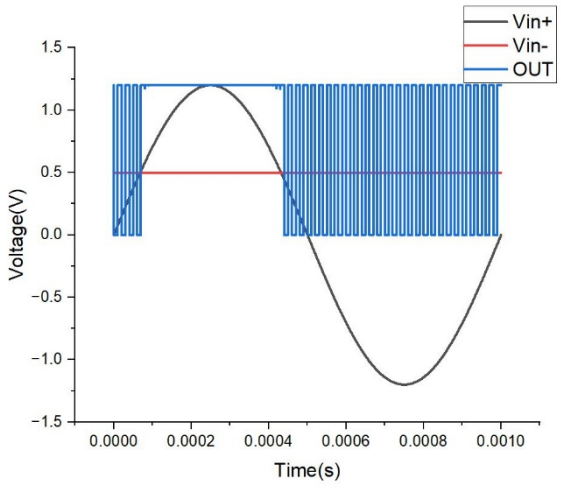

Fig.5. Simulation of the Comparator output

For the transient simulation a sinusoidal signal of 1KHz is applied as Vin+ and 500mV of DC signal is used for Vin- .A clock signal of frequency 20K is being applied.

The power consumption of the propsed comparator is to be measured.For this , the proposed circuit was simulated under 90nm CMOS technology with 1.2V supply.Under the aforementioned conditions,the circuits consumes an average of 4.598 micro watt power.The relation between the VDD and the power dissipation is also verified graphically(Fig.6).From the graph it is clear that as the VDD increases the power consuption increases proportionally.

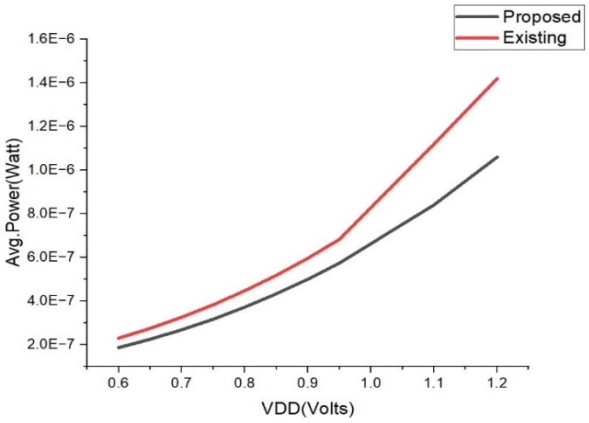

Fig.6. Supply voltage Vs Power

The propsed design consumes less power compared to the existing designs.The supply voltage is varied from 0.6V to 1.2 V and the behaviour of power dissipation is plotted.In all these ranges the new design out performs the existing design in terms of power consumption.

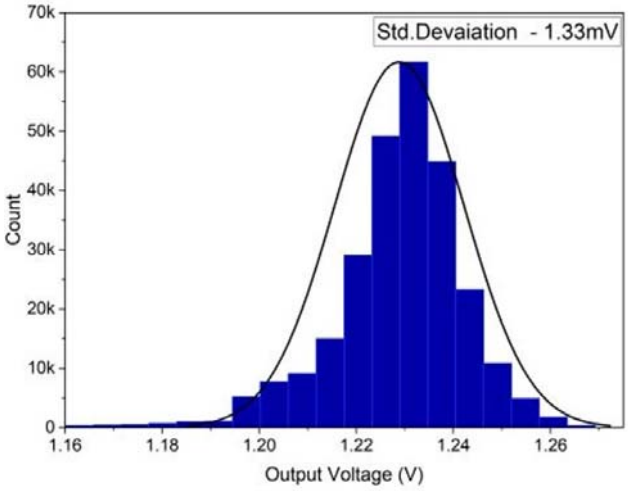

Fig.7. Monte carlo simulation

The monte-carlo analysis of the propsed design is conducted for 250 runs.The offset voltage of the design is found to be 1.33mV.This value is lesser than the offset voltages of the contemporary architectures.This proves the accuracy and linearity of the circuit.The histogram result is shown in Fig.7.The new design out performs the existing designs in terms of power dissipation and simplicity.Design simplicity is achieved by using only 11 number of transistors in the circuit.

Delay Analysis and comparison

The delay of a two stage dynamic comparator can be generally expressed as shown eq.1

$$T_{delay} = T_{latch} + T_{pre-amp} \quad (1)$$

T_{delay} is the total delay of the comparator. T_{latch} is the term which represents the time for completing the latching operation. $T_{pre-amp}$ is the time taken by the amplification stage to complete the operation.The delay of this circuit is found in the simuation as 39.26ps .It is comparable with other similar designs.

Table 1. Comparison chart for different comparators

Paper	[9]	[10]	[11]	This work
Technology	90	90	90	90
Supply	1	1	1	1
Power (uW)	32.6	31.8	48.23	4.538
Delay (ps)	54.5	26.9	20.95	39.26
No.of Transistors	13	12	18	11

The proposed work is compared to the existing work to qualitatively analyse the design (Table.1).Amongst the listed works, the presented comparator consumes the least power.The offset voltage of the newly designed architecture is also better compared to the existing design.The circuit function is acheived with minimum number of transistors(11 number of transistors only used).Transistor count of the proposed design is less.The design simplicity is achieved by using only 11 number of transistors in the circuit.

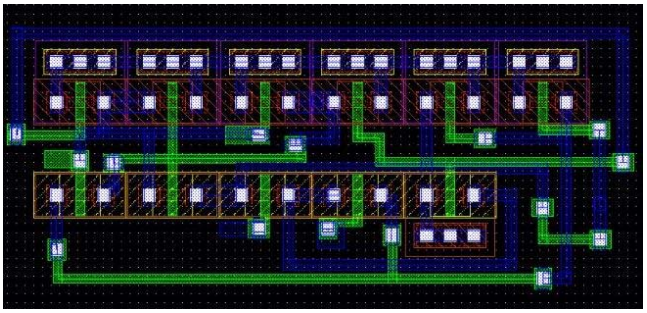

Fig.8. Simulation of the Comparator output

The layout of the designed comparator is given in Fig.8.The area of the die is found as 20.76um^2.This result proves the simplicity of the design.The acheived die size is smaller than the existing ones.

Conclusion

In this study,a low power low offset dynamic two stage single tail comparator is realised.The comparators are essential for the design of data convertor systems.The implantable devices are using data convertors for the digitilisation of the biosignals.The durabilty of such battery operated systems depend on the power consumption.In ADC, dynamic comparator is one of the biggest power consumer.This study proposes a novel comparator, which consumes least power and with less circuit complexity.Die area of the proposed work is less than many reported works.Another advantage of this design is the low offset voltage.This proves the linearity of the device.Considering the above points,this methodology can be used to design the dynamic comparator for the implantable biomedical devices.

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