

# Design and Implementation of High Precision Four Channels up to 100MHz Frequency Meter and Pulse Generator Using FPGA

**Abstract.** The frequency counter, also called frequency meter, is an auxiliary tool for measuring the frequencies of digital signals, which often requires high measurement accuracy, which counts the number of cycles entered per second. These devices are widely used in designing electronics and telecommunications to measure wave frequency. In this paper, a high-precision 4-channel frequency meter up to 100MHz with an error rate of 0% was designed and implemented in addition to a liquid crystal display (LCD) to display the value of the input frequency to be measured and up to 100MHz pulse generator also for the system testing without the need to use an external pulse generator using (SPARTAN 3E-XC3S500 FPGA).

**Streszczenie.** Częstotliwościomierz, zwany też częstościomierzem, jest narzędziem pomocniczym do pomiaru częstotliwości sygnałów cyfrowych, co często wymaga dużej dokładności pomiaru, która zlicza ilość wprowadzonych cykli na sekundę. Urządzenia te są szeroko stosowane w projektowaniu elektroniki i telekomunikacji do pomiaru częstotliwości fal. W tym artykule zaprojektowano i wdrożono bardzo precyzyjny 4-kanalowy miernik częstotliwości do 100 MHz ze stopą błędów 0% oraz wyświetlacz ciekłokrystaliczny (LCD) do wyświetlania wartości mierzonej częstotliwości wejściowej i do 100MHz generator impulsów również do testowania systemu bez konieczności stosowania zewnętrznego generatora impulsów z wykorzystaniem (SPARTAN 3E-XC3S500 FPGA). (Projektowanie i wdrażanie wysoce precyzyjnego czterokanałowego miernika częstotliwości do 100 MHz i generatora impulsów z wykorzystaniem układu FPGA)

**Keywords:** FPGA, Frequency, DCM, MUX

**Słowa kluczowe:** FPGA, DCM, MUX, miernik częstotliwości

## Introduction

As time has progressed, the electronics industry has rapidly developed, and digital frequency meters are now playing a more important role in modern industrial production and scientific research, such as in the aerospace and electronics fields [1]. Frequency is a crucial parameter that reflects system stability in certain control and communication systems [2]. By understanding the frequency of a system at a given moment, we can predict its state at the next moment and take corresponding measures to improve system reliability. However, the choice of frequency meter can affect measurement accuracy, and high-precision frequency meters are widely used due to their small size, fast response speed, and high precision. In recent years, frequency measurement methods have evolved and become more accurate with the widespread use of high-precision frequency meters. However, there are still limitations in measurement accuracy for low and high frequencies. The counter synchronous parallel counting method was developed to address these limitations, but it has not significantly improved logical resource use for high precision [3].

FPGA devices were created in the 1980s and have since become a new type of reconfigurable high-performance computing hardware with applications in various fields. While they have been successful in aerospace and defense systems, voice recognition, image processing, and digital signal processing, they are only now beginning to enter control systems. Compared to traditional CPU-centered control systems, FPGA devices have superior dependability and can be updated at a faster rate. However, they also require a HDL implementation and may produce designs that exceed the capabilities of a particular FPGA [4].

Digital frequency meters are evolving towards integration and downsizing, and conventional architecture typically involves a CPU and an FPGA chip working together [5].

## Literature Review

In 2007, M. J. Moure and his team created a single FPGA chip that combined the steps of frequency measurement and mass resolution calculation. The system

was made more efficient and less complex with parallel processing, pipeline stages, and prediction techniques. The result was a low-cost, adaptable QCM sensor system that could function independently and had communication capabilities. The system was tested using a Xilinx Virtex-4 FPGA and a QCM sensor for electrochemical purposes in a damping environment [6].

In 2011, Hu Bing and Liu Xijun introduced a design for a digital frequency meter that was based on System-on-a-Programmable-Chip (SOPC) technology. The design was centered on the Cyclone series FPGA and had an 8051 IP core as its microcontroller. The frequency meter generated its desired frequency using the Bresenham algorithm and employed both frequency measurement and weak measurement techniques. It had a frequency range of 0.1Hz to 10MHz and was highly compact and efficient, with all main logic functions on a single chip, making it a valuable application of SOPC technology in industrial design [7].

In 2012, Yi-Yuan Fang and Xue-Jun Chen presented a design for a frequency meter that was more precise than traditional methods. The system was implemented using Altera's FPGA chip EP2C35F672C8 and was able to measure frequencies with equal precision and low measurement error throughout its entire frequency range [8].

In 2014, Peng Wang and others proposed a frequency meter that had equal precision and addressed the limitations of traditional frequency meters. The system, which consisted of an FPGA and a microcontroller, had consistent precision and accuracy across its full measurement range. It not only measured frequency but also performed real-time detection of period, pulse width, and duty ratio. The technical specifications of the system were as follows [9]:

The frequency measurement range was from 0.1 Hz to 50 MHz with a relative error of  $10^{-6}$  throughout the entire range.

1. The period measurement range was from 0.02  $\mu$ s to 1 s with a relative error of  $10^{-6}$ .

2. The pulse width measurement range was from 0.1  $\mu$ s to 1 s.

3. The duty ratio measurement range was from 1% to 99%.

In 2016, HUANG Rui published a study that looked at both traditional frequencies measurement methods that use analog circuit frequency characteristics and digital pulse counting frequency measurement methods. He analyzed the direct frequency measurement method and the cycle frequency measurement principle method to determine the cause of  $\pm 1$  count errors [10].

In 2018, Xiaoliang Fu and colleagues created a frequency and phase detector and counter based on FPGAs. The device was designed as a daughter board for the LLRF control system and connected to the motherboard using mixed signal connectors. The frequency error data was sent to a PC via a VXI data bus, and two analog phase error outputs were provided. In this design, a single unit was able to handle four channel discriminations of RF frequencies and phases. Testing showed that the phase detector had a bandwidth of 400 MHz, and a resolution of 1 Hz could be achieved through precise frequency discrimination. The phase-frequency detector was used in the Accelerator Cryo Module (ACM) system and met the requirements of the LLRF control system. Its stability and reliability were confirmed after extended use [11].

In 2018, Haobin Dong proposed a high-precision and fast-sampling frequency measurement method using FPGAs that improved the equal precision measurement technique. By linking FPGA carry chains with a delay line through serial full adders, the frequency measurement precision was increased while reducing counting errors. The results showed that the frequency resolution was 0.014 nT, with a relative error of under  $2 \times 10^{-6}$  at a sampling rate of 500 Hz, which represented significant improvements in precision and sampling rate for resonant frequency measurement [12].

In 2020, C. Manjula and D. Jayadevappa presented two new Processor Clock Signal Presence Detectors that utilized Edge Detection. They tested the functionality of processors and memories using the FCSRE, which was based on a multi-channel and programmable DPG. The results showed the incoming clock frequency, maximum binary count, number of lit LEDs, and simulation waveform of all sub-modules, along with FPGA demo snapshots of the FCSRE. A DLA test methodology was demonstrated, and the setup of the final experiment was described in detail, along with its main outcomes [13].

In 2022, Carlos Jiménez Fernández and colleagues carried out a study that involved a set of laboratory sessions for students to learn how to create clocks on FPGAs and determine the highest frequency that can be achieved. The circuit design was kept simple and allowed the use of an internal clock signal generation block, leading to a higher clock frequency than the input signal. The results of the study were found to be effective in teaching students the concept that internal signals can operate at much higher frequencies compared to external signals that may have limited frequency capabilities [14].

Also in 2022, Xinglin Sun and co-authors developed a high-precision frequency measurement system that addressed the problem of a 1-word quantization error. The system consisted of two parts: a rough measurement stage that used equal precision measurement and a precise measurement stage that utilized negative feedback tracking with a phase-frequency detector (PFD) and direct digital synthesizer (DDS). Both simulations and experiments confirmed the system's effectiveness and practicality, and with a 2 kHz sampling rate, the frequency measurement accuracy was improved by over 30 dB [15].

## Proposed system architecture

The system consists of several processors linked together to form the proposed system for measuring the input frequency and then displaying its value on the liquid crystal screen. The functioning of each part of the system will be explained in the following paragraphs.

- LCD (Liquid Crystal Display):** The Spartan-3E FPGA Starter Kit board is a 2-line by 16-character liquid crystal display (LCD). The 4-bit data link seen in Fig. 2 is used by the FPGA to drive the LCD. The Starter Kit board utilizes a 4-bit data interface even though the LCD offers an 8-bit data interface in order to maintain compatibility with other Xilinx development boards and to reduce the overall number of pins.

When used effectively, the LCD can show a variety of data using both bespoke and regular ASCII characters. These displays are slow, nevertheless. The display is slow in comparison to the board's 50 MHz clock. The LCD connection with FPGA shown in Fig. 1, while the interface character LCD interface signals are displayed in Table 1. [16].

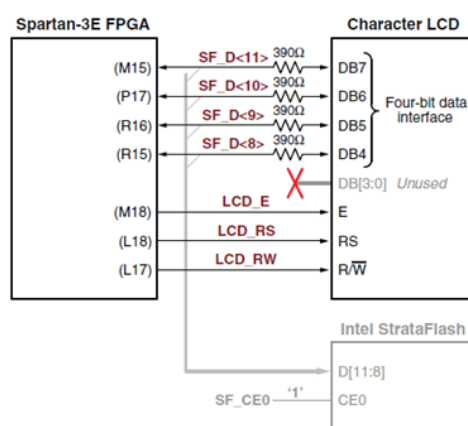


Fig. 1: LCD (Liquid Crystal Display)

Table 1: Character LCD Interface

Signal Name	FPGA Pin	Function
SF_D<11>	M15	Data bit DB7
SF_D<10>	P17	Data bit DB6
SF_D<9>	R16	Data bit DB5
SF_D<8>	R15	Data bit DB4
LCD_E	M18	Read/Write Enable Pulse 0: Disabled 1: Read/Write operation enabled
LCD_RS	L18	Register Select 0: Instruction register during write operations. Busy Flash during read operations 1: Data for read or write operations
LCD_RW	L17	Read/Write Control 0: WRITE, LCD accepts data 1: READ, LCD presents data

- DCM (Digital Clock Manager):** It is on the shelf component built in FPGA that used to control system designed maximum frequency and for other purpose by dividing or multiplying the default frequency by a factor. In the proposed system, there is two DCMs, first was used to multiply FPGA default frequency (50MHz) by 2 to obtain (100MHz) and the second was used to divide the output frequency of the first DCM by 2 to obtain (50MHz) [17].

- Pulse generator:** The pulse generator consists of a frequency divider that is calibrated through the rotary encoder through its calibration. The output frequency is selected by changing the number to be divided by the frequency, which is from (1Hz to 100MHz). Four push buttons are used to select increment or decrement step (10, 100, 1000 or 10000 Hertz) to reduce setting time for

calibrating the factor. The value to be divided by the frequency is displayed on the liquid crystal display (LCD), which is used to system testing and obtains the required frequency to enter it into the frequency meter and check the efficiency of the system. Since the default FPGA frequency is 50MHz, it is necessary to duplicate the frequency to obtain 100MHz using the first (DCM: Digital Clock Manager). Fig. 2 shows the block diagram of a variable frequency pulse generator and Digital Clock Manager (DCM). Second DCM is used to divide the output frequency of the first DCM by 2 to obtain (50MHz) through (g\_clk) signal to use in the most processes in the system designed. Note that needs two DCMs one for multiplying 50MHz by 2 to obtain 100MHz and other to divide output frequency (100MHz) outputted by the first DCM by 2 to obtain (50MHz) instead of using the original FPGA clock (50MHz) for the clock divider and other system processes because that using the same clock was denied by ISE synthesizer.

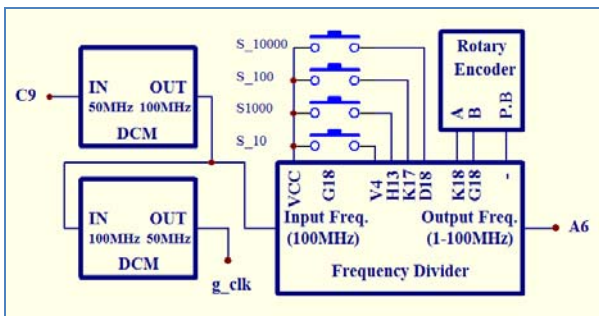


Fig. 2: Frequency Divider and Digital Clock Manager (DCM)

- **Channel selector:** Using 4-1 Multiplexer to select clock input channel from the outside signal to one of the four channels and then to measure its frequency via system designed. Fig. 3 illustrates 4-1 Multiplexer used for this purpose.

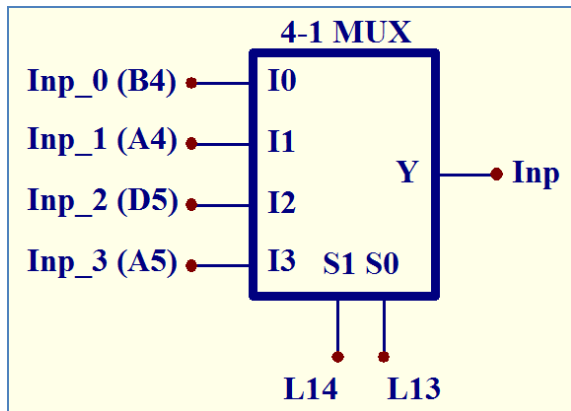


Fig. 3: Input Channel Selector

- **Frequency counter process:** In this process, the frequency of input signal will measure by count its number of falling edge or rising edge during one second calculated by another process that count  $50 \cdot 10^6$  clock cycle (2FAF080 in Hex) because of the system global clock as mentioned in Fig. 1 was 50MHz. The number of clock cycles of selected input signal via 4-1 MUX mentioned in Fig. 3 is counted in BCD (12 digit: up to 100,000,000,000 Hz) to display its value in decimal after convert all digits of this value to ASCII code and then send to the its proper location in LCD. Fig. 4 illustrates a block diagram of frequency counter with LCD 1602.

Fig. 5 shows the flowchart of the frequency counter process of the system design, while Fig.6 illustrates frequency meter timing diagram.

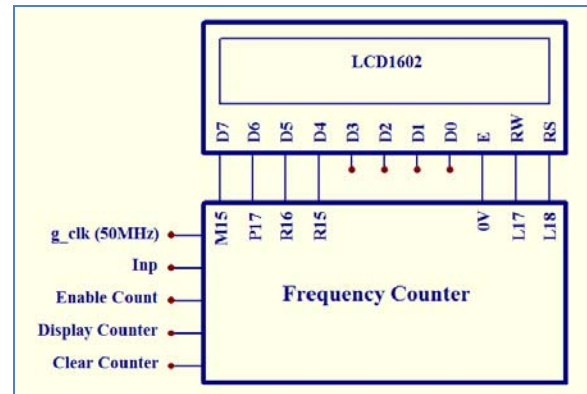


Fig. 4: Block Diagram of Frequency Counter with LCD1602

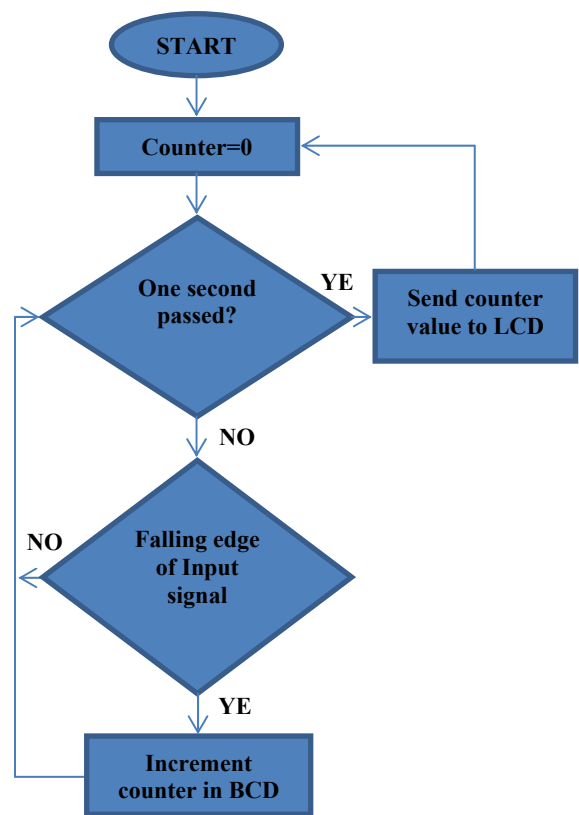


Fig. 5: Frequency counter flowchart

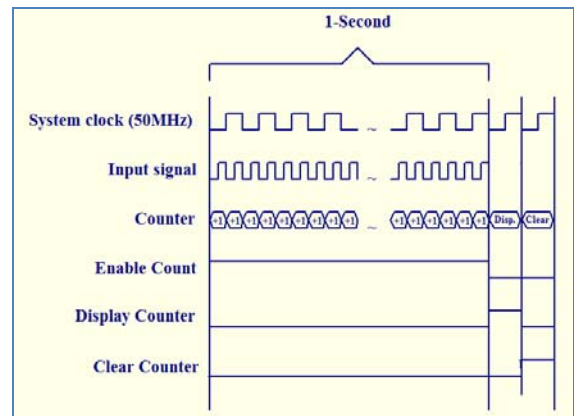


Fig. 6: Frequency counter timing diagram

## Results

Instead of using external pulse generator, embedded pulse generator was used to test system design and to show the accuracy of the measurement. From the following figures it is shown that the error is 0%.

Fig. 7 shows that the factor of the divider is 1 and input frequency to the frequency divider is 100MHz, then the output frequency is 100MHz, then the measurement value is shown in LCD is 100MHz exactly through channel\_0.



Fig. 7: Input frequency (100MHz) to Channel\_0

Fig. 8 illustrates that the factor of the divider is 2 and input frequency to the frequency divider is 100MHz, then the output frequency is 50MHz, then the measurement value is shown in LCD is 50MHz through channel\_0.



Fig. 8: Input frequency (50MHz) to Channel\_0

Fig. 9 illustrates that the factor of the divider is 3 and input frequency to the frequency divider is 100MHz, then the output frequency is 33.3333MHz, then the measurement value is shown in LCD is 33.3333MHz through channel\_0.



Fig. 9: Input frequency (33.3333MHz) to Channel\_0

Fig. 10 illustrates that the factor of the divider is 100 and input frequency to the frequency divider is 100MHz, then the output frequency is 1MHz, then the measurement value is shown in LCD is 1MHz through channel\_0.



Fig. 10: Input frequency (1MHz) to Channel\_0

Fig. 11 illustrates that the factor of the divider is 10 and input frequency to the frequency divider is 100MHz, then the output frequency is 10MHz, then the measurement value is shown in LCD is 10MHz through channel\_0.



Fig. 11: Input frequency (10MHz) to Channel\_0

Fig. 12 illustrates that the factor of the divider is 10000 and input frequency to the frequency divider is 100MHz, then the output frequency is 10KHz, then the measurement value is shown in LCD is 10KHz through channel\_0.



Fig. 12: Input frequency (10KHz) to Channel\_0

Fig. 13 illustrates that the factor of the divider is 50000000 and input frequency to the frequency divider is 100MHz, then the output frequency is 2Hz, then the measurement value is shown in LCD is 2Hz through channel\_0.



Fig. 13: Input frequency (2Hz) to Channel\_0

Fig. 14 illustrates that the factor of the divider is 1000000 and input frequency to the frequency divider is 100MHz, then the output frequency is 100Hz, then the measurement value is shown in LCD is 100Hz through channel\_0.



Fig. 14: Input frequency (100Hz) to Channel\_0

Fig. 15 illustrates that the factor of the divider is 100 and input frequency to the frequency divider is 100MHz, then the output frequency is 1MHz, then the measurement value is shown in LCD is 1Mz through channel\_1.



Fig. 15: Input frequency (1MHz) to Channel\_1

Fig. 16 illustrates that the factor of the divider is 100 and input frequency to the frequency divider is 100MHz, then the output frequency is 1MHz, then the measurement value is shown in LCD is 1Mz through channel\_2.



Fig. 16: Input frequency (1MHz) to Channel\_2

Fig. 17 illustrates that the factor of the divider is 100 and input frequency to the frequency divider is 100MHz, then the output frequency is 1MHz, then the measurement value is shown in LCD is 1Mz through channel\_3.



Fig. 17: Input frequency (1MHz) to Channel\_3

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## REFERENCES

- Juan Li , Fenxian Tian and Xinxin Sun, "Design and Implementation of a High Precision Frequency Meter based on Multimode", Advances in Computer Science Research (ACSR), volume 90, 3rd International Conference on Computer Engineering, Information Science & Application Technology (ICCIA 2019)
- Nemat A. A high-resolution digital frequency meter for low frequencies [J]. IEEE Transactions on Instrumentation & Measurement, 1990, 39(4):667.
- Li J, Ma X. The Design of Wide Input Range and High-Precision Frequency Meter Based on FPGA[C]// International Conference on E-product E-service & E-entertainment. 2010
- Sardar Masud Rana, Md. Anzan-Uz-Zaman, et-al, "Study on the Application of FPGA Based Frequency Counter Using VHDL Program with Nexus Board", *IE-42/VLSI-1, OCTOBER 2013*
- Haixin Sun, Yujie Fan and Qiang Xiang, "Design of SOPC digital frequency meter based on MicroBlaze", Journal of Physics: Conference Series, Haixin Sun *et al* 2021 *J. Phys.: Conf. Ser.* 1732 012164
- M. J. MOURE, et-al, 2007, "AN FPGA-BASED SYSTEM FOR THE MEASUREMENT OF FREQUENCY NOISE AND RESOLUTION OF QCM SENSORS", Latin American Applied Research, 37:25-30 (2007)
- Hu Bing and Liu Xijun, 2011, "Design and Research of SOPC Embedded Digital Frequency Meter Based on FPGA", M. Zhu (Ed.): ICCIC 2011, Part V, CCIS 235, pp. 476–482, 2011. Springer-Verlag Berlin Heidelberg 2011
- Yi-Yuan Fang and Xue-Jun Chen, 2012, "Design of Equal Precision Frequency Meter Based on FPGA", *Engineering*, 2012, 4, 696-700 <http://dx.doi.org/10.4236/eng.2012.410089> Published Online October 2012 (<http://www.SciRP.org/journal/eng>)
- Peng Wang, et-al, 2014, "Frequency Meter with Equal Precision Based FPGA + MCU", *Applied Mechanics and Materials*, ISSN: 1662-7482, Vol. 614, pp 308-311
- HUANG rui, 2016, " Design and Implementation of FPGA-Based Digital Frequency Meter", 6th International Conference on Machinery, Materials, Environment, Biotechnology and Computer (MMEBC 2016)
- Xiaoliang Fu, et-al, 2018, "400MHz FREQUENCY/PHASE DETECTOR AND COUNTER", 9th International Particle Accelerator Conference, ISBN: 978-3-95450-184-7m doi:10.18429/JACoW-IPAC2018-THPAK106
- Haobin Dong, et-al, 2018, "A high-precision and fast-sampling frequency measurement method based on FPGA carry chain for airborne optically pumped cesium magnetometer", 89(7):075001.doi: 10.1063/1.5036822.
- C. Manjula and D. Jayadevappa, 2020, "FPGA BASED CLOCK FREQUENCY SENSOR AND RANGE ESTIMATING SYSTEM FOR TESTING MEMORIES AND PROCESSORS", International Journal of Electrical Engineering and Technology (IJEET), Volume 11, Issue 5, July 2020, pp. 11-21, Article ID: IJEET\_11\_05\_002
- Carlos Jiménez Fernández, et-al, 2018, "FPGA design example for maximum operating frequency measurements", Authorized licensed use limited to: Universidad de Sevilla. Downloaded on January 26, 2022 at 11:34:55 UTC from IEEE Xplore. Restrictions apply.
- Xinglin Sun, et-al, 2022, "Frequency-Modulated Signal Measurement Using Closed-Loop Methodology", *Sensors* 2022, 22, 7822. <https://doi.org/10.3390/s22207822>, <https://www.mdpi.com/journal/sensors>
- Xilinx, "Spartan-3E FPGA Starter Kit Board User Guide", UG230 (v1.2) January 20, 2011
- "Using Digital Clock Managers (DCMs) in Spartan-3 FPGAs". xilinx.com