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Design of Fail-Safe Window Comparator Circuits Using Unconditional Deterministic Optimization

Abstract. *The window comparator circuit operates by comparing the input signal's level with a predetermined range of levels. If the signal falls within this specified range, the output will be set to a "High" logic signal; otherwise, it will be set to a "Low" logic signal. Fail-safe window comparator circuits find application in fault detection systems, particularly in scenarios that require high-precision and stable analog circuits. They are designed to be intrinsically safe, ensuring that in the event of any circuit failure, the output signal will consistently remain in a logical "Low" state. The design concept relies on an AND logic circuit that operates through transistor oscillation. This oscillation is determined by the specific values of resistances and input voltages. This paper introduces a methodology for designing fail-safe window comparator circuits across multiple voltage ranges. The approach involves optimizing the circuit's resistance values to accurately establish the boundaries of the upper and lower windows. This is achieved through the application of an optimization method that employs unconditional deterministic optimization techniques, specifically the maximum and minimum methods. The optimization conditions were assessed using the Scilab program, while circuit testing was conducted using the LTspice program.*

Streszczenie. *Obwód komparatora okienkowego działa na zasadzie porównywania poziomu sygnału wejściowego z określonym zakresem poziomów. Jeśli sygnał mieści się w tym określonym zakresie, wyjście zostanie ustawione na sygnał logiczny „wysoki"; w przeciwnym razie zostanie ustawiony na „niski" sygnał logiczny. Odporne na uszkodzenia obwody komparatorów okiennych znajdują zastosowanie w systemach wykrywania usterek, szczególnie w scenariuszach wymagających precyzyjnych i stabilnych obwodów analogowych. Zostały zaprojektowane tak, aby były samoistnie bezpieczne, zapewniając, że w przypadku jakiejkolwiek awarii obwodu sygnał wyjściowy będzie stale pozostawał w logicznym stanie „niskim". Koncepcja projektowa opiera się na obwodzie logicznym AND, który działa poprzez oscylację tranzystora. Oscylacja ta jest określona przez określone wartości rezystancji i napięć wejściowych. W tym artykule przedstawiono metodologię projektowania odpornych na uszkodzenia obwodów porównawczych okien w wielu zakresach napięcia. Podejście to obejmuje optymalizację wartości rezystancji obwodu w celu dokładnego ustalenia granic górnego i dolnego okna. Osiąga się to poprzez zastosowanie metody optymalizacji, która wykorzystuje bezwarunkowe techniki optymalizacji deterministycznej, w szczególności metody maksimum i minimum. Warunki optymalizacji oceniono za pomocą programu Scilab, natomiast testy obwodów przeprowadzono za pomocą programu LTspice. (**Projektowanie niezawodnych obwodów komparatorów okiennych z wykorzystaniem bezwarunkowej optymalizacji deterministycznej**)*

Keywords: fail-safe, window comparator, window detector, optimization.
Słowa kluczowe: fail-safe, komparator okien, detektor okien, optymalizacja.

Introduction

There exist two types of window comparator circuits: the analog window comparator and the digital window comparator. The analog window comparator operates as a feedback oscillator circuit, incorporating resistors and transistors. The specific resistor values play a crucial role in defining the boundaries of the window. However, a constant resistance value cannot universally accommodate all window boundaries, necessitating the adjustment of each resistance value to achieve the desired outcome [1-4]. The digital window comparator circuit employs comparator or op-amp module ICs, combining two distinct comparators with an AND logic gate [5]. In the Schmitt-trigger circuit, the application of logic gates with input hysteresis necessitated the use of eight transistors for the window comparator [6]. Handling low-voltage and rapidly changing inputs involved utilizing an XOR gate in conjunction with a potential divider circuit [7]. This type of window comparator, which incorporates digital logic ICs, relies on the comparison of digital switching voltage levels. Specifically, it compares the threshold voltages of CMOS Schmitt-trigger inverter logic and TTL AND logic gate [8]. In [9], a window comparator circuit was introduced, featuring digital switching levels. This circuit exhibits its efficacy in handling rapidly changing input signals at low voltages. It utilizes a combination of a voltage divider circuit with a resistor and an N-channel MOSFET. The design is based on the threshold voltage characteristics of CMOS logic ICs.

When comparing analog window comparators with digital window comparators, the analog window comparators exhibit the advantage of greater stability. However, they are accompanied by drawbacks such as slower response speeds and increased complexity in circuit design. Both types of circuits share a common design principle, involving the establishment of a window boundary with well-suited upper and lower voltage signal thresholds [10-14].

Mathematical optimization of a function involves determining either its maximum or minimum value [15]. This could refer to the highest or lowest point of the function. Specifically, a relative maximum signifies the highest value within a given point, surpassing its neighboring points. Conversely, a relative minimum denotes the lowest value within a specific point, falling below its neighboring points. Optimization finds relevance in various applications, including tasks like designing analog electronic circuits [16-19] or in the assessment of other electronic circuits like power electronics [20-21].

Based on the aforementioned concepts, this study introduces a design for an analog window comparator circuit. This design employs an optimization approach that identifies the suitable resistance values required to establish the upper and lower window boundaries. This optimization process leverages unconditional deterministic optimization techniques, specifically the maximum and minimum methods. The optimization conditions were evaluated using the Scilab program, while the performance of the circuit was tested using the LTspice program.

The Window Comparator Circuits and Optimization Method

A. Fail-Safe window comparator circuits

The fundamental principle of the window comparator circuit involves comparing the input signal level with a predefined range of levels. When the signal is situated within this predetermined range, the output registers a "High" logic signal. Conversely, if the signal falls outside this range, the output reflects a "Low" logic signal. The window comparator circuit is also recognized for its hysteresis voltage characteristic. The fail-safe window comparator, illustrated in Fig. 1, was introduced and applied within fail-safe industrial applications [4].

The design concept revolves around generating feedback transistor oscillation using an AND logic circuit. This oscillation is influenced by the resistor values and input voltages of each AND input, coupled with a pump-up circuit. The AND inputs are confined within a predetermined voltage window boundary, which enables the AND gate output to function as the output for the fail-safe window comparator [4]. Analog fail-safe window comparator circuits find utility in applications such as digital fail-safe counters, fail-safe relay drivers, and circuits necessitating the detection of various safety signals utilizing the pump-charge circuit.

The design concept relies on generating feedback transistor oscillation through the utilization of an AND logic circuit. This oscillation is determined by the specific resistor values and input voltages associated with each individual AND input, as depicted in Fig. 2.

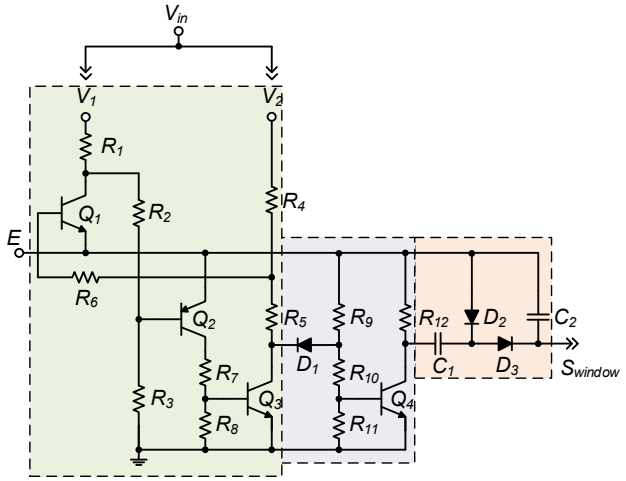

Fig. 1. The Fail-safe window comparator circuit [4].

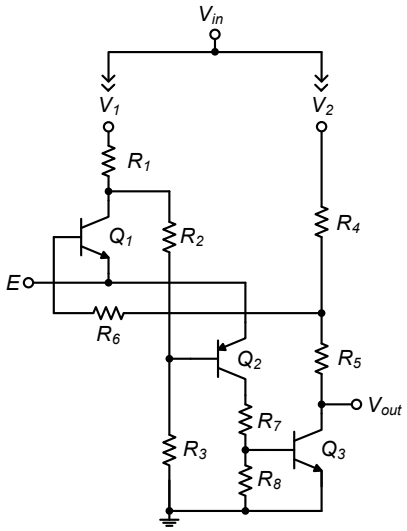

Fig. 2. The analog window comparator circuit [1-4].

This represents a fail-safe approach applied to prevent the detection of faults arising from different issues, specifically by monitoring voltage levels within a defined window boundary. The circuit employs transistors Q_1, Q_2, and Q_3 in the feedback oscillation process. When an input voltage is applied to Vin, the oscillation occurs in a sequence of states: Q_2 off, Q_3 off, Q_1 on, Q_2 on, Q_3 on, and Q_1 off, respectively. The equation (1) serves to establish the window boundary or the voltage level window.

$$\frac{R_4 + R_5}{R_5} \cdot E \; > \; V_{in} > \frac{R_1 + R_2 + R_3}{R_3} \cdot E \tag{1}$$

From equation (1), it defines the region of the window, ensuring that the input signal falls within this designated range, as illustrated in Fig. 3.

B. Optimization Method

Optimization represents a multifaceted and non-linear engineering solution that relies on a combination of expertise, logical deduction, trial and error, and the scientific method to aid decision-making. The principle of optimization involves a numerical computational procedure that strives to yield the optimal numerical value for a given problem. This entails employing various techniques to attain outcomes through mathematical modeling, objective functions, constraints, and optimization criteria.

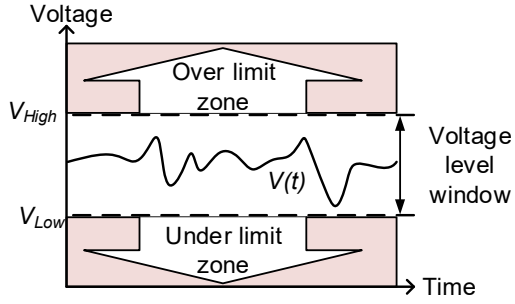

Fig. 3. Voltage window boundary [4].

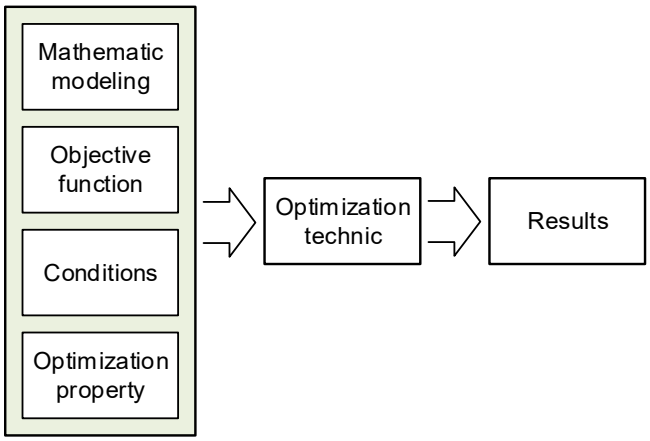

Fig. 4. Elements of Optimization

An unconditional optimization refers to a problem that exclusively involves unconditional objective function with a gradient vector, as Equations (2) and (3).

$$\nabla y_n = 0 \tag{2}$$

$$\frac{dy}{dx_1} = 0, \frac{dy}{dx_2} = 0, \ldots, \frac{dy}{dx_n} = 0 \tag{3}$$

From equation (3), the critical point, where the derivative equals zero, is referred to as the extremum point,

which can manifest as either a relative maximum or a relative minimum.

Simulation results and discussion

A. *Scilab Optimization Program Code*

The algorithm design follows the diagram in Fig. 4, defining mathematical modeling from Equation 1, objective functions for circuit elements, conditions for some resistance values for initial values, and optimization properties for circuit input.

```
// window comparator (window boundary with DC source)
clc;
e_input = 5.0;                  // (volt) input supply voltage
v_low_side = 8.0;               // (volt) low side voltage input
v_high_side = 14.0;             // (volt) high side voltage input
va_low = v_low_side;            // (volt) fix value of input voltage
vb_low = e_input-(0.7);         // (volt) fix output voltage Q2 on
R3 = 15000;                     //(ohm) fix output resistance (R3)
rb_low = R3;
ra_low = ((va_low/vb_low)* rb_low)-rb_low;
r2 = 2200;                      //(ohm)fix R2
R1 = ra_low-r2                  //(ohm) find R1 (R1=Ra_low-R2)
R2 = r2
va_high = v_high_side;          // (volt) fix value of input voltage
vb_high = e_input+(0.7);        // (volt)fix output voltage Q1 on
R5 = 2200;                      // (ohm) fix output resistance (R5)
rb_high = R5;
ra_high = ((va_high/vb_high)*rb_high)-rb_high;
R4 = ra_high                    //(ohm) R4 from above procedure
ex = 5:1:15
in_V1 = (R1+R2+R3)*(ex/R3)
in_V2 = (R4+R5)*(ex/R5)
// end
```

The result of the Program Code.

```
R1  = 10706.977
R2  =  2200.
R3  = 15000.
R4  = 3203.5088
R5  = 2200.
 ex  =
   5.   6.   7.   8.   9.   10.   11.   12.   13.   14.   15.

 in_V1  =
   9.3023256   11.162791   13.023256   14.883721   16.744186
18.604651   20.465116   22.325581   24.186047   26.046512
27.906977

 in_V2  =
   12.280702   14.736842   17.192982   19.649123   22.105263
24.561404   27.017544   29.473684   31.929825   34.385965
36.842105
```

Determine the value of the resistance by selecting the resistance value that is actually used, by resistor R1 is 10000 ohms and resistor R4 is 3300 ohms to find window boundary.

```
R1  = 10000;
R2  = 2200;
R3  = 15000;
R4  = 3300;
R5  = 2200;
ex = 5:1:15
in_V1 = (R1+R2+R3)*(ex/R3)
in_V2 = (R4+R5)*(ex/R5)
in_V1  =
   9.3023256   11.162791   13.023256   14.883721   16.744186
18.604651   20.465116   22.325581   24.186047   26.046512
27.906977

in_V2  =
   12.280702   14.736842   17.192982   19.649123   22.105263
24.561404   27.017544   29.473684   31.929825   34.385965
36.842105
```

B. *Circuit Simulation with LTspice*

Circuit simulation with Ltspice using the conditions from the previous section. From Table 1, setting DC voltage source 8 volts to get a window boundary between 14.5 - 20 volts.

Table. 1. The window boundary level range adjusts according to the level of supply voltage.

E	Window Boundary	
	V_1 (Volts)	V_2 (Volts)
5	9.06	12.50
6	10.88	15.00
7	12.69	17.50
8	14.50	20.00
9	16.32	22.50
10	18.13	25.00
11	19.94	27.50
12	21.76	30.00
13	23.57	32.50
14	25.38	35.00
15	27.20	37.50

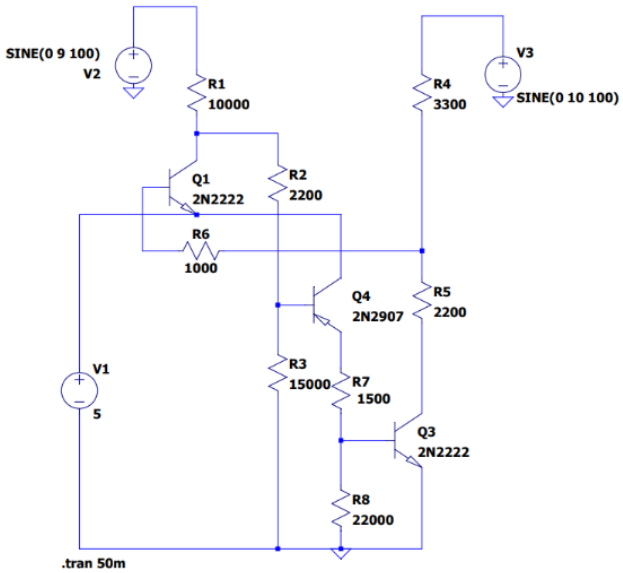

Fig. 5. LTspice simulation program

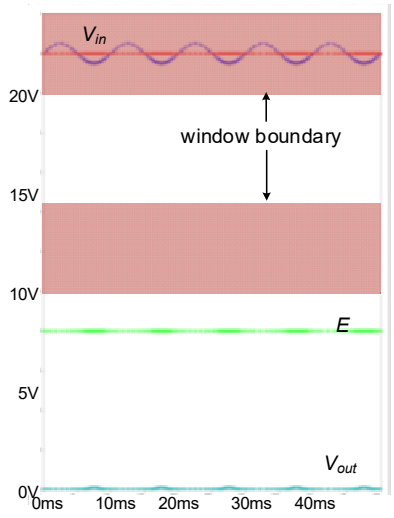

Fig. 6. Results of simulation with DC input over boundary.

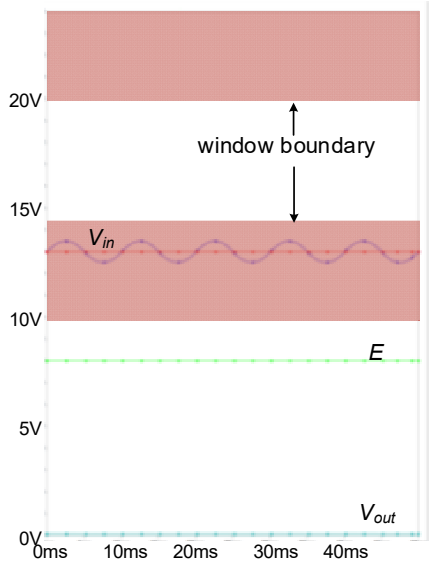

Fig. 7. Results of simulation with DC input under boundary.

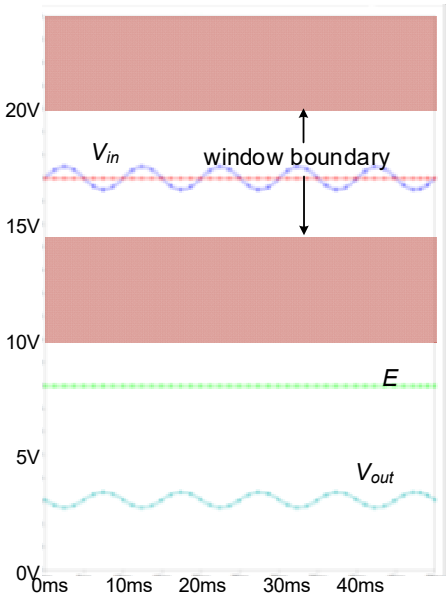

Fig. 8. Results of simulation with DC input within boundary.

C. *Discussion*

Windows comparator circuit testing to determine the window boundary from the DC voltage source in the resulting optimization method. Finding the most suitable resistance value to determine the window boundary. The resistance value that is not practical must be set and close to the appropriate resistance value and then substituted in the equation again. Relation between the DC power supply voltage and the window boundary, an example is shown in Table 1. Fig. 5-8 is a simulation of a computer program by setting 8 volts DC voltage source to the window boundary of 14.5-20 volts.

It can be concluded that using the optimization method in analog window comparator design can be done by defining mathematical modeling conditions, objective functions, conditions, and optimization properties to obtain practical results.

Conclusions

This paper presents a method for designing an analog circuit with multiple difficult design conditions by optimization method. The window comparator circuits in various voltage ranges by determining the resistance of the circuit by an optimization method, that find the appropriate resistance to determine the boundaries of the upper and lower windows by using the maximum and minimum method using unconditional deterministic optimization. Optimization conditions were tested with the Scilab program and circuit test with the LTspice program.

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